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Index

S.No.	Experiment	Page No.
1.	Colour Code of Resistor	04
2.	Conversion of galvanometer into voltmeter	08
3.	Conversion of galvanometer into ammeter	10
4.	Temperature coefficient of resistance of thermistor	12
5.	Frequency response of R-C circuit - Low-pass	16
6.	Frequency response of R – C circuit - High-pass	19
7.	L-C-R Series and parallel Resonance	22
8.	Maximum power transfer theorem	27
9.	Thevinin's theorem	29
10.	Norton's theorem	33
11.	De Sauty's bridge	37
12.	Anderson's bridge	39
13.	Wein's bridge -Filter circuit	41
14.	CRO voltage & frequency measurement	43
15.	CRO - Phase measurement	46
16.	Frequency response of R – L circuit (Low-pass)	49
17.	Frequency response of R – L circuit (High-pass)	52
18.	P-N Junction Diode	55
19.	Zener Diode	59
20.	Rectifiers and filters	62

21.	Bipolar junction transistor – Characteristics	68
22.	Field effect transistor – Characteristics	73
23.	Unijunction transistor – Volt –Ampere characteristics	79
24.	Silicon Controlled rectifier	84
25.	Unijunction transistor – Relaxation Oscillator	88
26.	R-C Coupled Amplifier	92
27.	Hartley Oscillator	96
28.	Colpitt's Oscillator	99
29.	Operational Amplifier as inverting amplifier	102
30.	Schmitt's Trigger	106
31.	Astable Multivibrator	110
32.	Operational amplifier 741 as a stable multivibrator	114
33.	Operational amplifier 741 as differentiator	119
34.	Operational amplifier 741 as monostable multivibrator	124
35.	Operational amplifier 741 as Wein bridge Oscillator	129
36.	Amplitude modulation and detection	133

1. Colour Code of Resistor

<u>Aim</u>: - To study the system of colour coding which is used to indicate the resistance value of carbon resistors. To measure the resistances of different resistors by colour code system and compare these values with those that measured with multi-meter.

Apparatus:-Carbon resistors and multi-meter.

<u>Description</u>: Fixed carbon composition resistors are too small in size to have the value of resistance to print on them. So a system of colour coding is used to indicate their resistances in Ohms. The colours used in the code and the number they represent are indicated in the table. Specification of a resistance can be found by using this colour-coding table. Three colours are sufficient to identify the values of resistors. The fourth band ,if any, gives the tolerance.

<u>Theory</u>:- <u>First method</u>:- The body colour of resistor indicates the first digit of resistance, one end or tip indicates the second digit and the dot colour near the center of the resistor represents the number of zeros following the first two digits (fig 1)

<u>Second method</u>: - The colour bands painted on the body of the resistors indicate the values. The colour bands are read from left to right from one end, which has the band closure to it. (fig 2)

The first three bands give the resistance value. The first and second bands indicate the first and second significant digits while the third band gives the number of zeros , which follows the first two digits. In case the third band is gold or silver, it represents a multiplying factor of 0.1 or 0.01 respectively. If however the third band is black, it means, do not add zeros to the first two digits. The resulting number is the resistance in ohms.

The fourth band represents the error in value called tolerance. If the fourth band is gold, it means a tolerance of $\pm 5\%$, where as fourth band is silver means a resistance of tolerance of $\pm 10\%$. Absence of fourth band means a resistance of tolerance of $\pm 20\%$.

<u>For five bands</u>: The first three bands represent the usual resistance of the resistor. The first and second bands indicate the digits and the third band indicates the number of zeros following the two digits. The fourth band gives tolerance. The fifth band gives reliability

level. The colour code for reliability is, Brown -1%, Red -0.1%, Orange -0.01%, Yellow -0.001% and so on.

The first band close to one edge indicates the first digit in the numerical value of the resistor.

<u>Procedure</u>:- First the resistance of the given resistor is measured according to the colour code system, including tolerance and this is verified with the value measured by digital multimeter by keeping its band switch in proper resistance range. The values are to be noted in the in the table-2.

Precautions: -

- 1) Care should be taken in deciding the first edge.
- 2) Tolerance can also be taken into consideration while measuring resistance as per colour code.

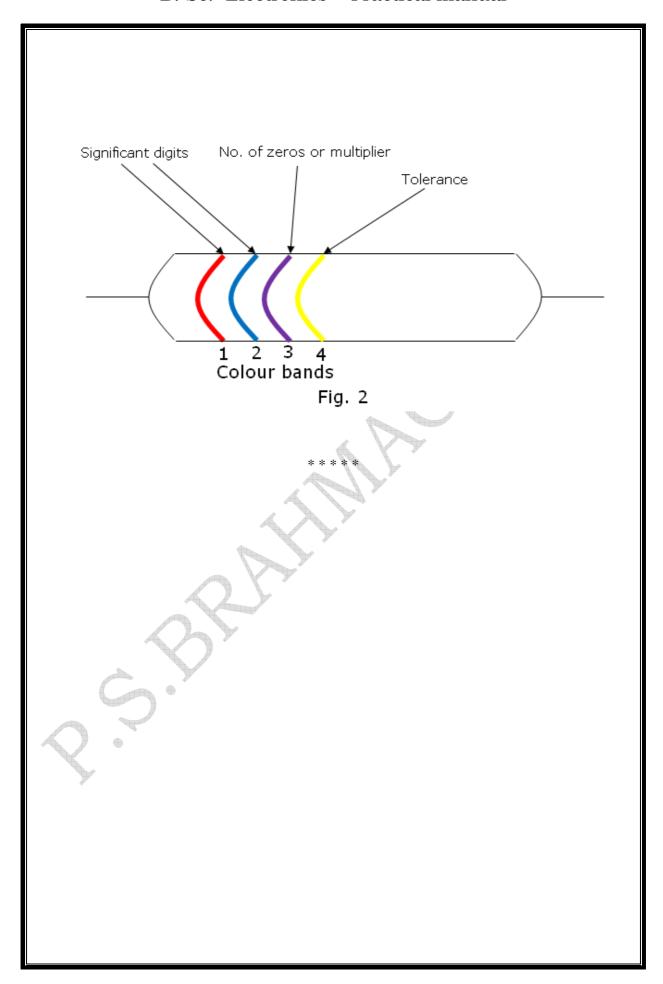
Result: -

Table- 1

S.No.	Colour	Value	Colour
1.	Black	0	
2.	Brown	1	
3.	Red	2	
4.	Orange	3	
5.	Yellow	4	
6.	Green	5	
7.	Blue	6	
8.	Violet	7	
9.	Grey	8	
10.	White	9	

S.No	I Band	II Band	III Band	IV Band	Value of	Resistance
					Resistance	Measured with
					(Ω)	Multi-meter
						(Ω)
1.						
2.						
3.					4	
4.						
5.						
T:	colou	r B	ody col	our	Dot colo	ur
Пр				g. 1		

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Page 7

2. Conversion of galvanometer into voltmeter

<u>Aim</u>: - To convert galvanometer into voltmeters of different ranges which can be used to measure the potential differences in electrical circuits.

<u>Apparatus</u>: - Galvanometer, voltmeter, variable resistor, variable power supply and connecting terminals.

Description: - A galvanometer can be converted in to a voltmeter by connecting a high resistance (R) in series with the galvanometer as shown in the figure. The value of resistance (R) connected in series decides the range of the voltmeter. The scale is calibrated in volts, so as to read the potential difference directly. To measure the potential difference between two points, the voltmeter must be connected in parallel across those two points in the circuit. When a high value of resistance is connected in series to the galvanometer, only a small fraction of the total current will flow through the galvanometer. So, this does not cause any damage to the galvanometer. More over, as the current flow in the galvanometer, which is connected in parallel in the circuit, is very small, it causes no effect in the current of the main circuit.

Procedure: - Connect the circuit as shown in the figure. The variable power supply connected gives the required potential difference to the circuit. Also select and connect the required resistance (R) in series with the galvanometer, to convert the galvanometer into voltmeter of required range. The selection of the resistance that should be connected in series to the galvanometer is in such away that the galvanometer shows full deflection for the required range. By increasing the supply voltage, the galvanometer reading is increased in steps of 5 divisions, starting from zero, the corresponding voltmeter readings are noted, in the table.

Graph: - A graph is drawn, by taking galvanometer reading on X- axis and the corresponding voltmeter reading on Y-axis. It gives a straight line passing through the origin. The graph is useful to know the potential difference across any two points in the circuit if the galvanometer reading is known.

The experiment is repeated by connecting another resistance (R)in series with the galvanometer to get a voltmeter of a different range. So the same galvanometer can be used to get voltmeters of different ranges, just by changing the series resistance (R).

Precautions: -

- 1) The series resistance should be so selected such that for the required range of voltmeter, the galvanometer shows full the deflection with in the scale.
- 2) The continuity of connecting terminals should be checked before going to the experiment.

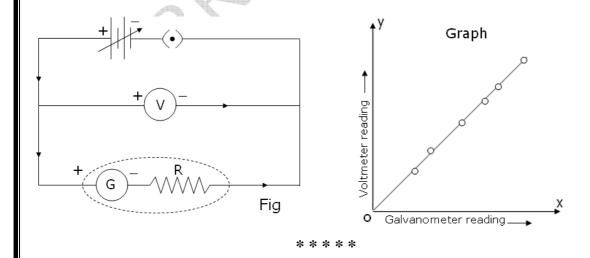
Results: -

Table

Voltmeter range = V

Value of resistance connected in series to galvanometer = Ω

S.No.	Galvanometer reading	Voltmeter reading	
	(n divisions)	(V)	
1.		7	
2.			
3.			
4.			
5.			



3. Conversion of galvanometer into ammeter

<u>Aim</u>: - To convert galvanometer into ammeters of different ranges which can be used to measure the currents in electrical circuits.

<u>Apparatus</u>: - Galvanometer, ammeter, rheostat, variable power supply, different shunt (variable) resistors and connecting terminals.

Description: - A galvanometer is a device used to detect the flow of the current, but not to measure. Because its scale is not marked in amperes, though its deflection is proportional to the current. Being the sensitive instrument, galvanometer cannot be used to measure large currents, because it may cause damage to the coil of the galvanometer. In order to avoid this damage and to use it as an ammeter, a low resistance is connected in parallel to the galvanometer. As a result, even if a large amount of current is sent in the main circuit, only a very small fraction of it passes through the galvanometer. The scale is calibrated in amperes, for the total current, so as to read the current directly. To measure the current, the ammeter must be connected in series in the circuit. The value of shunt resistance (R_s) depends upon the fraction of the total current required to pass through the galvanometer.

Procedure: - Connect the circuit as shown in the figure. The variable power supply connected gives the required potential difference to the circuit, to send the required current through the ammeter. Also select and connect the required shunt resistance R_s , across or parallel to the galvanometer, such that the galvanometer shows full deflection for the required range of current. Then the galvanometer is said to be converted into an ammeter of required range. By increasing the supply voltage, the galvanometer reading is increased in steps of 5 divisions, starting from zero, the corresponding ammeter readings are noted, in the table.

Graph: - A graph is drawn, by taking galvanometer reading on X-axis and the corresponding ammeter reading on Y-axis. It gives a straight line passing through the origin. The graph is useful to know the current in the circuit, if the galvanometer reading is known.

The experiment is repeated by connecting another shunt resistance (R_s) to get the ammeter of a different range. So the same galvanometer can be used to get ammeters of different ranges, just by changing the shunt resistance (R_s).

Precautions: -

- 1) The shunt resistance (R_s) should be so selected such that for the required range of ammeter, the galvanometer shows full deflection with in the scale.
- 2) The continuity of connecting terminals should be checked before going to the experiment.

Results: -

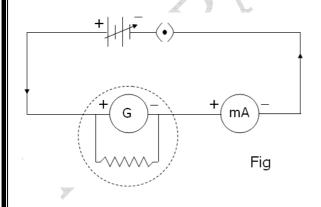
Table

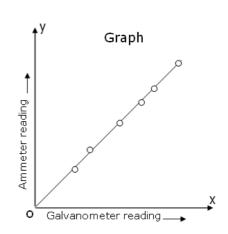
Ammeter range =

mA Shunt resistance added =

Ω

S.No.	Galvanometer reading	Ammeter reading
	(n divisions)	(mA)
1.		
2.		
3.		
4.		
5.		





* * * * *

4. Temperature coefficient of thermistor

<u>Aim</u>:- To determine temperature coefficient of resistance of the given thermistor and also to draw the V - I characteristic curve.

<u>Apparatus</u>: Post office box, thermistor, galvanometer, battery, plug-key, rheostat, thermometer, hot water bath, voltmeter, milli - ammeter and connecting terminals.

Formula:- The temperature coefficient of resistance of the given thermistor

$$\alpha = \frac{S_2 - S_1}{S_1 t_2 - S_2 t_1} / {}^{0}c$$

Where S_1 and S_2 are the resistances of the thermistor at temperatures $t_1^{\,o}C$ and $t_2^{\,o}C$ respectively.

Description:- Thermistor is a heat sensitive resister usually made up of a semi-conducting material, such that its resistance varies appreciably with change in temperature. Thus the thermistor has a large temperature coefficient of resistance. They may have negative or positive temperature coefficient. The high sensitivity to temperature changes makes the thermistor extremely well-suited for the precise temperature measurement, control and compensation. Hence, they are widely used for such purposes, particularly in the lower temperature range of -100 °C to +350 °C.

Thermistors are made by sintering mixtures of metallic oxides such as Mananese, Cobalt and Copper etc. Their resistance varies from 0.5 Ω to 100 M Ω . These are chemically stable. These can be connected in series or parallel, depending up on the purpose.

The V- I curve is not a straight line. So it is a non-linear or non- ohmic resister. As the current increases, first the voltage increases and then decreases.

Procedure:- a) Temperature characteristic curve:

The circuit is connected as shown in the figure-1 using Post office box. In P and Q arms 100Ω and 10Ω resistances are taken(in general) and in S arm the thermistor is connected. If the connections are correct, the galvanometer shows opposite deflections for the resistance (R) values of zero and infinite respectively. Initially at room temperature the bridge is balanced by adjusting R and the resistance (S) of the thermistor is calculated using the formula

$$\frac{P}{Q} = \frac{R}{S}$$

Now the thermistor is kept in a water bath and the temperature is increased from 30° C to 90° C, in steps of 5° C. At every temperature the bridge is balanced by adjusting the R-value and the S value is calculated. The experiment is repeated while decreasing the temperature also.

<u>Graph</u>: A graph is drawn by taking temperature on X- axis and resistance of the thermistor on Y- axis (figure-2). For two close and different values of t_1 and t_2 , the corresponding resistances S_1 and S_2 are taken. The values are substituted in the formula given below and obtain the temperature coefficient of resistance of the thermistor.

$$\alpha = \frac{S_2 - S_1}{S_1 t_2 - S_2 t_1} / {}^0c \quad \text{which is negative}$$

b) <u>Voltage- current characteristic</u>:- The circuit is connected as shown in the figure-3. The current is varied in the circuit by adjusting the jockey position of the rheostat and the potential across the thermistor is measured for each value of current. The current and potential difference values are noted in the table-2. The voltage first raises and then falls with increase of current.

Graph: A graph is drawn by taking current on X- axis and voltage on Y-axis, as shown in the figure- 4 and studied how the voltage varies with increase of current.

Precautions:-

- 1) The resistances P and Q should be maintained at constant values.
- 2) Much current should not be sent through the thermistor.
- 3) First we have to observe whether the galvanometer shows opposite deflections or not for the resistance (R) values of zero and infinite respectively.

Results	:-		

$$P=100\;\Omega$$

$$Q = 10 \Omega$$

S.No.	Temperature °c	Resistance (R) Ω	Thermistor Resistance (S) = $\frac{Q}{P} xR$
1.			
2.			
3.			. 4 \ 7
4.			
5.			
6.			
7.			
8.			
9.			
10.			

Table-2

S.No.	Current (I)	Voltage (V)
600	(mA)	V
1.		
2.		
3.		
4.		
5.		

 $_{
m Page}15$

5.Frequency response of R-C circuit

(Low-pass)

<u>Aim</u>: - To observe the frequency response of an R –C circuit, which behaves as a low pass filter circuit and to find the upper 3-db (cut-off) frequency.

<u>Apparatus</u>: - Signal generator, AC milli – voltmeter, connecting terminals, a series combination of resistance and capacitance.

<u>Formula</u>:- The upper 3-db(cut-off) frequency $f = \frac{1}{2\pi RC} Hz$

Where R = Resistance in the circuit (Ω)

 $C = Capacitance in the circuit (\mu F)$

Voltage gain
$$G = \frac{e_0}{e_i}$$

 e_o = Out put voltage (V)

 $e_i = In put voltage (V)$

Description and theory:- The R-C filter circuit passes low frequency a.c. readily. The resistance of the resistor is independent of the applied AC frequency. But in case of capacitor, as the frequency increases, the reactance ($X_c = 1/\omega C$) of the capacitor decreases. At low frequencies, the capacitor acts as open circuit, as the reactance is very high. So at this lower frequencies as $X_c \gg R$, the P.D. across the capacitor is also high compared to that across the resistor. So the total input (e_i) component appears at the out put(e_0) i.e. across the capacitor. Also the total of the p.d's across the resistor and capacitor is equal to e_i .

As the frequency of the AC signal increases the reactance of the capacitor decreases and the potential difference (e_0) across the capacitor also decreases as X_c decreases. But at very high frequencies i.e. in M Hz, the capacitor virtually short-circuited and the out put (e_0) across the condenser falls to zero.

Procedure: - Connect the circuit as shown in the figure. In this circuit one end of R is connected to C and the other end is connected to the signal generator. The second terminal of the capacitor is connected to the other terminal of the signal generator. The out put (e_0) is measured across the condenser by a.c milli voltmeter.

Keep the input voltage (e_i) at constant value (1V) and vary the frequency of AC signal generator from 10 Hz and so on, up to M Hz and note down the values of out put voltage(e_0) using AC milli-voltmeter and calculate the gain ($G = e_0/e_i$) for all values of frequencies and note down the gain ratio in the observation table.

(Note:- To measure the out put voltage, digital multi-meter should not be used. Because at higher frequencies i. e. above 5 K Hz it shows less values instead of actual values.)

<u>Graph</u>: A graph is plotted between frequency and gain, by taking the frequency or $\log f$ on x – axis and gain on y – axis. This is called frequency response curve. The frequency and gain characteristics are as shown in the figure. The frequency corresponding to 0.707 times to the maximum gain (0.707G_{max}) is noted. It is the upper 3-db(cut-off) frequency.

Precautions:-

- 1) The continuity of the connecting wires should be tested first.
- 2) The frequency of the signal generator should varied from the lowest value.

Result: - The frequency corresponding to 0.707 times to the max gain $(0.707G_{\text{max}})$ and the frequency from the formula $f = \frac{1}{2\pi RC} Hz$ are equal. i.e. the upper 3-db frequency from graph and from formula are equal.

 $_{\rm Page}17$

6. Frequency response of R – C circuit (High-pass)

 \underline{Aim} : - To observe the frequency response of a R – C circuit, which behaves as a high pass filter circuit and to find the lower 3-db(cut-off) frequency.

<u>Apparatus</u>: - Signal generator, AC milli – voltmeter, connecting terminals, a series combination of resistance and capacitance.

<u>Formula</u> :- **<u>Formula</u>** :- The lower 3-db(cut-off) frequency $f = \frac{1}{2\pi RC} Hz$

Where R = Resistance in the circuit (Ω)

C = Capacitance in the circuit (μF)

Voltage gain
$$G = \frac{e_0}{e_i}$$

 e_o = Out put voltage (V)

 $e_i = In put voltage (V)$

Description and theory: - In order to understand the frequency response of C-R circuit, a sinusoidal input is applied to the C-R circuit. The resistance of the resistor is independent of the applied AC frequency but the reactance of capacitor ($X_c = 1/ωC$) decreases with the increase of frequency. At low frequency the capacitor offers high reactance and the current flowing through the circuit is less. So the P.D. across the resistor is less or the attenuation is more. Similarly, as the frequency increases, the reactance of the capacitor decreases and the current flow in the resistor as well as the P.D. across it increases. At very high frequencies the reactance X_c is so small that the capacitor C acts almost as a short circuit and virtually all the inputs appears at the output i.e. across the resistor. Thus this behaves as a high pass circuit.

Procedure: - Connect the circuit as shown in the figure. The input is taken from the signal generator and output is measured across the resistor using a AC milli-voltmeter. Keep input voltage (e_i) constant and vary the frequency from 10Hz to 1MHz and note down the corresponding values of output voltage (e_o) and calculate the gain value ($G = e_0 / e_i$) for all values of frequencies and note down the gain ratio in the observation table.

(Note:- To measure the out put voltage, digital multi-meter should not be used. Because at higher frequencies i. e. above 5 K Hz it shows less values instead of actual values.)

<u>Graph</u>:- A graph is plotted between frequency and gain, by taking the frequency or $\log f$ on x – axis and gain on y – axis. The frequency and gain characteristics are as shown in the figure. The frequency corresponding to 0.707 times to the maximum gain (0.707 G_{max}) is noted. It is the lower 3-db(cut-off) frequency.

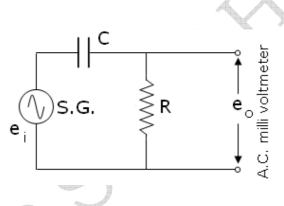
Precautions: - 1) The continuity of the connecting wires should be tested first.

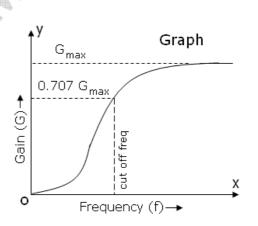
2) The frequency of the signal generator should varied from the lowest value.

Result: - The frequency corresponding to 0.707 times to the max gain (0.707 G_{max}) and the frequency from the formula $f = \frac{1}{2\pi RC} Hz$ are equal. i.e. The lower 3-db(cut-off) frequency from graph and from formula are equal.

The input voltage $e_i = 1V$

S.No.	Frequency (Hz)	Out put voltage (e ₀) (V)	Voltage gain $G = \frac{e_0}{e_i}$	Log f
1.				10 Y
			4	
				# · · · · · · · · · · · · · · · · · · ·
20.				





* * * * *

7. L-C-R Series and parallel Resonance

<u>Aim</u>: To study the frequency response and to find resonant frequencies of L-C-R series and parallel circuits. Also to find the quality factor and band width in L-C-R series circuit.

<u>Apparatus</u>: A variable non-inductive resistor, a variable capacitor, a variable inductor, a signal generator, an a.c. milli- ammeter and the connecting wires.

<u>Formula</u>:- The resonance frequency $f_0 = \frac{1}{2\pi LC}$ Hz

Where L = Self inductance (mH)

 $C = Capacity of the capacitor (<math>\mu F$)

Quality factor
$$Q = \frac{2\pi f_0 L}{R}$$

Where $R = Resistance (\Omega)$

Band width = $(f_2 - f_1)$ (Hz)

Also Quality factor
$$Q = \frac{f_0}{f_2 - f_1}$$

Where f_1 and f_2 are the frequencies at the half power points.

<u>Description and theory</u>:- (Series L-C-R) When the resistor R, inductor L and capacitor C are connected in series with a source of emf E, the circuit is called as the series resonant or series tuned circuit (figure-1). This is an acceptor circuit, that means it allows maximum current to flow through it at a particular (resonant) frequency and at all other frequencies it allows less current.

In A.C. circuits the voltage and the current are usually out of phase. Across the inductor, the current lags behind the voltage by 90^{0} , where as across the capacitor, the current leads the voltage by 90^{0} . But across the resistor the voltage and current both are in phase. Under certain conditions, the voltage and current are in phase, even though the circuit consists of L , C and R and the circuit behaves as a pure resistor. This phenomenon is called resonance. This occurs at a single frequency known as resonant frequency. At this frequency the capacitive reactance($X_c = 1/\omega C$) and the inductive reactance($X_L = \omega L$) are equal and opposite in direction. So they get cancelled each other and only resistance acts.

The impedance of the circuit is given by $Z = R + j (\omega L - 1/\omega C)$

At resonance the reactive term disappears $\omega L - 1/\omega C = 0$

The impedance is minimum i.e. Z = R

The current is maximum I = E/R

So $\omega L = 1/\omega C$

$$\omega_0 = \omega = 2\pi f_0 = \frac{1}{\sqrt{LC}}$$

At this frequency the current is maximum and this frequency f_0 is called resonant frequency. The circuit has selective properties. To compare selectivity or sharpness of resonance, a band of frequencies is chosen at which the current falls to $\frac{1}{\sqrt{2}}$ times (half power points) of its maximum value. The frequency difference $(f_2 - f_1)$ between the half power points is called the bandwidth.

<u>L-C-R parallel</u>: Parallel resonant circuit (figure-2) is one in which one branch consists of an inductor L with associated resistor R and the other branch consists of a capacitor C. This is a rejector circuit, that means it rejects the current or allows minimum current to flow through it, at a particular (anti- resonant) frequency and it allows more current at all other frequencies. So the circuit is not selective. But it is highly selective when energized from a high impedance generator.

The impedance of the circuit is given by

$$\frac{1}{Z} = \frac{1}{R + j\omega L} + \frac{1}{\frac{1}{j\omega C}}$$

At resonance the impedance is maximum.

The impedance at resonance $Z = \frac{L}{CR}$

The anti-resonance frequency $f_o = \frac{1}{2\pi} \sqrt{\frac{1}{IC} - \frac{R^2}{I^2}} H_Z$

If R-value is small, then $f_0 = \frac{1}{2\pi \sqrt{IC}}$ Hz

Procedure:- For L-C-R series, the circuit is connected as shown in the figure-1. The source resistance and the series resistance should be small. The out put voltage of the signal generator is adjusted to be around 5V. The frequency of the signal generator is changed in steps and the corresponding current values are noted from the a.c. milli- ammeter. The readings are tabulated. The current values increase with the increase of frequency, up to the resonant frequency, further increase of frequency causes the decrease of current. The L,C and R values are noted to calculate the resonant frequency f_0 and Q-factor, using the above formulae.

 $\underline{\text{Note}}$:- The experiment may be repeated with a different values of 'R'. Here the f_o value is un changed, but Q- factor value is changed.

Graph: A graph is drawn for current against frequency. The frequency corresponding to maximum current is noted and it is the resonant frequency f_0 . The frequencies f_1 and f_2 corresponding to half power points is noted and from it the bandwidth, $(f_1 - f_2)$ is noted. From the values of f_0 , f_1 and f_2 , the quality factor, Q is calculated.

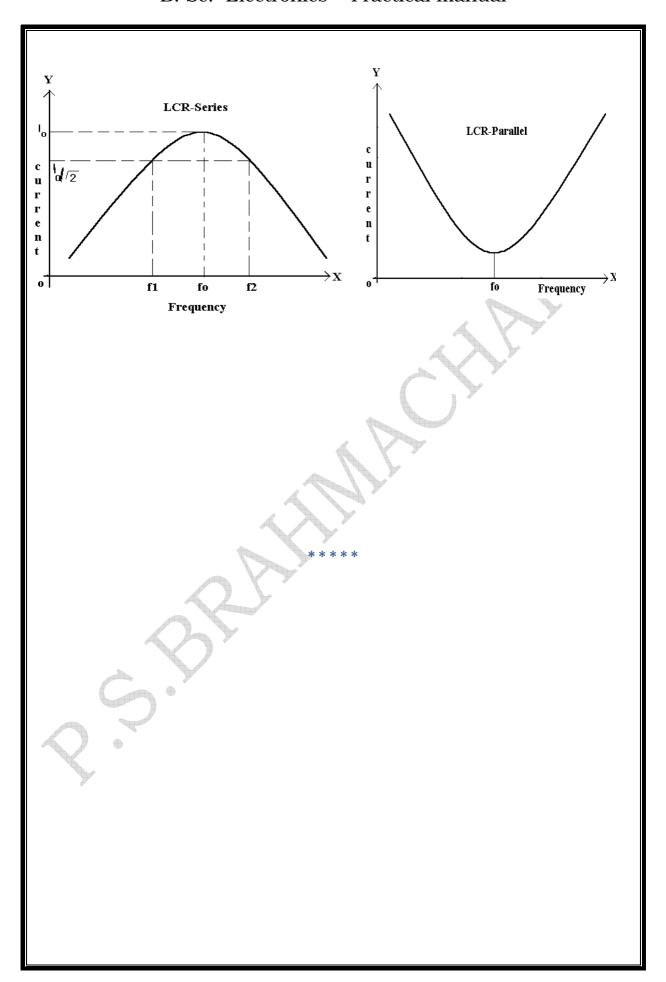
For <u>L-C-R parallel</u>, the circuit is connected as shown in the figure-2. The frequency of the signal generator is changed in steps and the corresponding current values are noted from the a.c. milli- ammeter. The readings are tabulated. But here, the current values decrease with the increase of frequency up to the anti- resonant frequency, further increase of frequency causes the increase of current. The anti- resonant frequency f_o is noted corresponding to the minimum current in the circuit.

<u>Graph</u>: A graph is drawn for current against frequency. The frequency corresponding to minimum current is noted and it is the anti-resonant frequency f_0 .

Precautions:-

Results:-

- 1) The internal resistance of the source and series resistance should be small.
- 2) Before going to the experiment the resonant frequency should be calculated from L and C values so that to select the range of frequencies for observation.



 $_{ ext{Page}}26$

8. Verification of maximum power transfer theorem

<u>Aim</u>:- To verify the maximum power transfer theorem.

<u>Apparatus</u>:- Battery, carbon (non-inductive) resistors, voltmeter, milli-ammeter, variable load resistor, multimeter and connecting terminals.

Formula: Power $P = I_L^2 R_L = V_L^2 / R_L$ watt

Where I_L = Load current.

 R_{L} = Load resistance.

 V_L = Voltage across the load

Description:-Maximum power transfer theorem states that "In two terminal a.c. net work the load will absorb maximum power from a generator if the load impedance is the complex conjugate of the internal impedance of the generator." But in d.c. circuit the load draws maximum power from the source, when the load resistance is equal to the internal resistance of the source i.e. at $R_L = R_S$ the power consumed by the load is maximum. The power in the load is given by $P = I_L^2 R_L$ (OR) V_L^2 / R_L .

Procedure:- The circuit is connected as shown in the figure-1. First the load is removed from the circuit. The battery is replaced by its internal impedance (Assume that the internal impedance is equal to zero and the terminals are short-circuited). The resistance between the terminals A and B is measured by using a multi-meter. It is the resistance of the source (R_S) . Now the battery and the load resistance R_L are connected in their places. By varying the value of R_L from $R_L < R_S$ to $R_L > R_S$, the voltage across the load and current through the load are noted. The values are tabulated as shown.

Now the power is calculated by using the formula $P = I_L^2 R_L$ (OR) V_L^2 / R_L for each value of current I_L or V_L . Take the value of R_L at the maximum power. If R_L value is equal to the internal resistance of source or generator R_S , then the theorem is proved.

<u>Graph</u>:-A graph is drawn between the power P and the load resistance R_L , as shown in the figure 2, by taking power P on Y- axis and load R_L on X - axis. The graph shows that the power is maximum when the load resistance is equal to the internal resistance of the source.

Precautions:

- 1) The load resistance R_L is varied from $\langle R_S \rangle$ to $\langle R_S \rangle$.
- 2) Internal resistance of the source should be measured before going to the experiment.
- 3) The battery should be removed and those terminals should be shorted while measuring the source resistance.

Results:-

,age 28

9. Thevinin's theorem

<u>Aim</u>:- To verify the Thevinin's theorem.

<u>Apparatus</u>:- Carbon resistors, battery, multi-meter, milli-ammeter, load resistor and connecting terminals.

Formula: - Load current
$$I_L = \frac{V_{th}}{R_{th} + R_L}$$
 mA

Where $V_{th} = \text{Thevinin's voltage}$ (V)

 $R_{th} = \text{Thevinin's resistance}$ (K\Omega)

 $R_L = \text{Load resistance}$ (\Omega)

Description: -To simplify the solutions of the complicated net works, many network theorems were developed. The vinin's theorem is one of them. The statement of this theorem is that "The current in a load impedance R_L , connected to a two terminal (A&B) net work of generators and impedances is same, if this load impedance R_L is connected to a single voltage generator, whose emf is the open circuit voltage (V_{th}) measured across A&B, connected in series with an impedance, which is equal to the impedance of the net work (R_{th}) between the same two terminals A&B, when all the generators in the net work have been replaced by their internal impedances."

<u>Figure -1</u> is the network containing number of generators and linear impedances. V_{th} is the open circuit (Thevinin's) voltage across A& B. R_{th} is the (Thevinin's) impedance between A & B, when the source is replaced by its internal impedance.

Procedure: The voltage source is disconnected and the terminals are short circuited, by assuming that the internal impedance of the voltage source is zero. And the resistance across A & B is measured after removing the load R_L . This resistance is the Thevinin's resistance R_{th} . Now the voltage source or battery is connected. The voltage across A &B is measured. This is the open circuit voltage and is called as Thevinin voltage (V_{th}). Now the load resistance R_L is connected in its place in series with a milli-ammeter or multi-meter and the current I_L through the load is measured. Similarly, the V_{th} and I_L are measured for different source voltages (V). The values V, V_{th} and I_L are noted in the <u>table-1</u>.

The circuit is replaced by a voltage source V_{th} with a series resistor whose value is equal to R_{th} . This is the Thevinin's equivalent circuit. Now the load R_L is also connected in series with a milli- ammeter between A & B. Then the current $I_L^{\ 1}$ through the load R_L is measured for different values of V_{th} noted in the <u>table-1</u>. These V_{th} and $I_L^{\ 1}$ values are noted in the <u>table-2</u>. It is observed that for same values of V_{th} in tables-1 and 2, the I_L and $I_L^{\ 1}$ are equal. Also calculate the I_L values using the above formula. These values are also equal to $I_L^{\ 1}$ Values.

Precautions: -

- 1) To measure V_{th} , the load R_L should be removed for each time.
- 2) The R_{th} computed should be nearly equal to the measured R_{th} value.

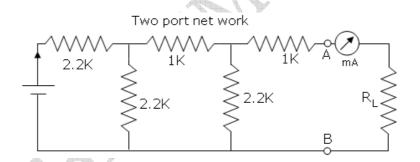
 $\frac{\textbf{Table-1}}{\textbf{R}_{th} \text{ measured across the terminals A and B}} = \textbf{K}\Omega$

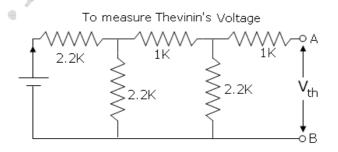
S.No.	Source	V_{th}	Load
	Voltage(V)	Measured	Current(I_L)
	V	V	mA
1.	42>		
2.			
3.			
4.	***		
5.			
6.			

 R_{th} computed = $K\Omega$

 R_L load resistance = $K\Omega$

S.No.	V _{th} Computed V	Load Current (I _L ¹) mA	Load Current(I_L) mA (From table .1)	$I_{L} = \frac{V_{th}}{R_{th} + R_{L}} \text{ mA}$ (Calculated I _L)
1.				42_7
2.				
3.				
4.				1
5.				7
6.				





32

10. Norton's theorem

Aim: - To verify the Norton's theorem.

<u>Apparatus</u>:- Carbon resistors, battery, multi-meter, milli-ammeter, load resistor and connecting terminals.

<u>Formula</u>:- The load current $I_L = \frac{I_N R_N}{R_N + R_L} mA$

Where $I_N = Norton's current$ (mA)

 R_N = Norton's resistance (K Ω)

 R_L = Load resistance (Ω)

Description: - To simplify the solutions of the complicated net works, many network theorems were developed. Norton's theorem is one of them. The statement of this theorem is that "The current (I_L) in a load impedance, connected to two terminals A & B of a network of generators and linear impedances is same if this load impedance is connected to a constant current generator, whose generated current (I_N) is equal to the short circuit current between the terminals A and B, in parallel with an impedance (R_N) equal to the impedance of the net work between the same two terminals A and B, when the generators in the net work have been replaced by their internal impedances."

<u>Figure-1</u> is the network containing number of generators and linear impedances. I_N is the short circuit (Norton's) current between A& B. R_N is the (Norton's) impedance between A & B, when the source is replaced by its internal impedance.

Procedure: - The voltage source is disconnected and the terminals are short circuited by assuming that the internal impedance of the voltage source is zero. And the resistance across A & B is measured after removing the load R_L . This resistance is the Norton's resistance R_N . Now the voltage source or battery is connected. The current between A &B is measured. This is the short circuit current and is called as Norton's current (I_N). Now the load resistor R_L is connected in its place in series—with a milli-ammeter or a multimeter and the current I_L through the load is measured. Similarly, the I_N and I_L are measured for different—source voltages (V). The values V, I_N and I_L are noted in the <u>table-1</u>.

The circuit is replaced by a constant current source I_N with a parallel resistor, whose value is equal to R_N . This is the Norton's equivalent circuit. Now the load R_L is also connected in series with a milli-ammeter between A & B. Then the current $I_L^{\ l}$ through the load R_L is measured for different values of I_N measured in the <u>table-1</u>. The I_N and $I_L^{\ l}$ values are noted in the <u>table-2</u>. It is observed that for same values of I_N in tables1 and 2, the I_L and $I_L^{\ l}$ are equal. Also calculate the I_L values using the above formula. These values are also equal to $I_L^{\ l}$ Values.

Precautions: -

- 1) To measure I_N , the load R_L should be removed for each time.
- 2) The R_N computed should be nearly equal to the measured R_N value.

<u>Result</u>: - The currents I_L and I_L^1 measured and calculated in tables 1 & 2 are equal for the same values of I_N .

 $\frac{\textbf{Table-1}}{R_N \text{ measured across the terminals A and B}} = K\Omega$

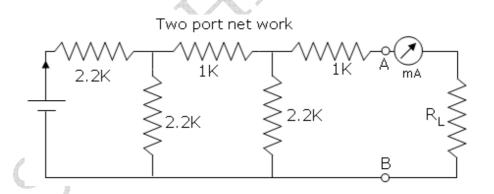
S.No.	Source	I_N	Load
	Voltage(V)	Measured	Current(I_L)
	V	mA	mA
1.			
2.			
3.			
4.			
5.			
6.			



 $R_N \text{ computed} = K\Omega$

 R_L load resistance = $K\Omega$

S.No.	I _N Computed mA	Load Current (I _L ¹) mA	Load Current(I _L) mA (From table .1)	$I_{L} = \frac{I_{N} R_{N}}{R_{N} + R_{L}} mA$ (Calculated I _L)
1.				42
2.				
3.				4 Ky
4.				
5.				1
6.				



To measure Norton's current

2.2K

1K

2.2K

2.2K

2.2K

3 B

36

11. De Sauty's bridge

<u>Aim</u>: To compare the capacities of two condensers (or) to find the capacitance of the given condenser, by using De Sauty's bridge.

<u>Apparatus</u>: Two condensers, two resistance boxes or two resistance pots of 10 KHz, Signal generator, head phone and well insulated connecting wires.

<u>Formula</u> :- Capacity of a unknown capacitor $C_2 = \frac{R_1}{R_2} x C_1$ µF

Where C_1 is the capacity of the known capacitor.

 R_1 and R_2 are the variable non-inductive resistors.

Description: The De Sauty's bridge is an A.C Bridge works on the principle of Wheat stone's bridge. This bridge is used to determine the capacity of an unknown capacitor C_2 in terms of the capacity of a standard known capacitor C_1 . Here R_1 and R_2 are non-inductive resistors. R_1 , R_2 , C_1 and C_2 are connected in a Wheat stone's bridge as shown in the figure-1. When the bridge is balanced, the ratios of impedances are equal as given below.

$$\frac{Z_1}{Z_2} = \frac{Z_3}{Z_4}$$

$$\frac{1}{\frac{j\omega C_1}{R_1}} = \frac{\frac{1}{j\omega C_2}}{R_2}$$

$$\frac{C_2}{C_1} = \frac{R_1}{R_2}$$

Procedure: The connections are made as shown in the figure. The resistance R_1 and a condenser C_1 are in series in one branch of the bridge and a resistance R_2 and another capacitor C_2 are in series in another branch. The A.C signal generator frequency is adjusted to a fixed value of 1 KHz or below, which is convenient to our ear.

A resistance is unplugged in R_1 and the resistance R_2 is adjusted till the sound in the head - phone is reduced to zero level . The value of R_2 is measured with a multi-meter and noted. While measuring the resistances, they should be in open circuit. The above process is repeated for different values of R_1 and the values are noted in the table .

When the hum in the head – phone is at zero level , then the time constants of the upper and the lower braches of Wheat stone's bridge equal i.e. $C_1R_1=C_2R_2$.

$$C_2 = \frac{R_1}{R_2} x C_1 \quad \mu F$$

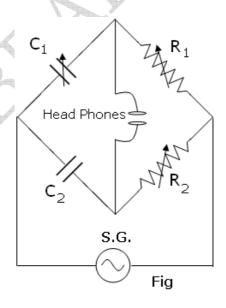
Precautions:-

- 1) The connecting wires should not be in contact with the experiment table.
- 2) The wires are checked up for continuity.

Result :-

Table

S.No.	Capacity of known condenser $C_1 \mu F$	Resistance $R_1 \Omega$	Resistance $R_2 \Omega$	Capacity of unknown condenser $C_2 = \frac{R_1}{R_2} X C_1 \mu F$	Standard Value of C ₂ µF
1.					
2.			4		
3.				7	
4.		A			
5.		4			
6.					



* * * * *

12. Anderson's bridge

Aim: - To measure the self - inductance of a given coil by Anderson's bridge method.

<u>Apparatus</u>: Inductor, standard capacitor, resistors (fixed resistances and variable pots as given in the circuit) signal generator, head phones and connecting terminals.

Formula: Inductance of given coil $L = C[(R_1 + R_2)R_5 + R_2R_4]$ mH

Where $C = Capacity of the standard capacitor (<math>\mu F$)

 $R_2, R_3, R_4 = Known$, fixed and non – inductive resistances (K Ω)

 R_1 , R_5 = Variable resistances ($K\Omega$)

<u>Description</u>: Anderson's bridge is the most accurate bridge used for the measurement of self – inductance over a wide range of values, from a few micro-Henries to several Henries. In this method the unknown self-inductance is measured in terms of known capacitance and resistances, by comparison. It is a modification of Maxwell's L - C bridge. In this bridge, double balance is obtained by the variation of resistances only, the value of capacitance being fixed.

Procedure:-The circuit diagram of the bridge is as shown in the <u>figure</u>. The coil whose self-inductance is to be determined, is connected in the arm AB, in series with a variable non-inductive resistor R_1 . Arms BC, CD and DA contain fixed and non – inductive resistors R_2 , R_3 and R_4 respectively. Another non - inductive resistor R_5 is connected in series with a standard capacitor C and this combination is put in parallel with the arm CD. The head - phones are connected between B and E. The signal generator is connected between A and C junctions.

Select one capacitor and one inductor and connect them in appropriate places using patch chords. The signal generator frequency is adjusted to audible range. A perfect balance is obtained by adjusting R_1 and R_5 alternatively till the head – phones indicate a minimum sound. The values of R_1 and R_5 are measured with a multi-meter(While measuring the R_1 and R_5 values, they should be in open circuit).In the balance condition the self – inductance value of the coil is calculated by using the above formula. The experiment is repeated with different values of C.

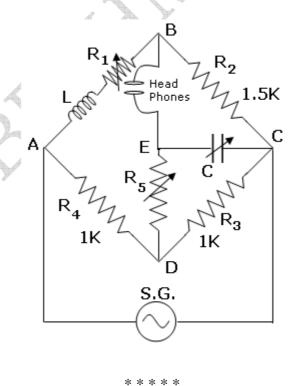
Precautions: -

- 1) The product (CR_2R_4) must always be less than L .
- 2) R_1 and R_5 are adjusted until a minimum sound is heard in head phones.

Result :-

7	<u>'a</u>	b	l	e

S.No.	Capacity (C) μF	Resistance (R_1) Ω	Resistance (R_5) Ω	$ \begin{array}{c c} Calculated \ value \ (L) & Standard \\ C \ [\ (R_1 + R_2 \) \ R_5 + R_2 R_4] & value \ of \ L \\ mH & mH \end{array} $
1.				
2.				
3.				
4.				
5.			4	
6.				



 $_{
m age}40$

13. Wein's bridge

(Filter circuit)

<u>Aim</u>: To study the frequency response of the Wein's bridge circuit, which is used as a frequency detector or filter circuit.

<u>Apparatus</u>: - Carbon resistors, capacitors, variable resistors(resistance box), signal generator and A.C. voltmeter.

Formula: - The anti-resonant frequency $f_0 = \frac{1}{2\pi RC} Hz$

quite sharp if $R_2 = 2R_4$.

Where $C = C_1 = C_3 = \text{Capacity of condenser } (\mu \text{ F})$

 $R = R_1 = R_3 = R_2 = Resistance$ (K\O)

(<u>Note</u>: - Here R_2 need not be equal to R_1 or R_3 . But $R_1 = R_3$, $C_1 = C_3$ and $R_2 = 2 R_4$ i.e. $R_4 = R_2/2$.)

Description: - Robinson modified the Wien's capacity bridge as filter circuit. This circuit works as a L-C-R parallel circuit or twin-T network i.e. it acts as rejector circuit. This Wein's bridge can be used to determine the frequency of an A.C. source (frequency detector). ABCD is the Wein's bridge filter circuit. A signal generator is connected between A and C, to study the frequency response and an AC voltmeter is connected across B and D to measure the output. The out put voltage is minimum at the frequency $f_0 = \frac{1}{2\pi RC}$. The minimum is

Procedure: - The circuit is connected as shown in the <u>figure</u>. Here R_1,R_2 and R_3 are fixed resistors each having a value equal to 2.2 K Ω and R_4 is a variable resistor (resistance box). First the value of ' f_0 ' is calculated by substituting R and C values in the above formula, to select the range of frequency that should be given in the signal generator. The input voltage from the signal generator is adjusted to 1V. Initially by selecting the frequency of the signal generator below the calculated f_0 value, its value is gradually increased in equal steps. For each frequency value the output voltage V_0 is measured across B and D by using an AC voltmeter or multi-meter. First the out put voltage V_0 decreases and then raises with increase of frequency. The output voltage is minimum at the anti-resonant frequency (f_0).

<u>Graph</u>: A graph is drawn by taking frequency (f) on X- axis and output voltage (V_o) on Y-axis. The out put voltage first decreases and then increases with increase of frequency. The frequency corresponding to minimum voltage is noted and it is the anti- resonant frequency f_o . This is equal to the calculated anti-resonant frequency.

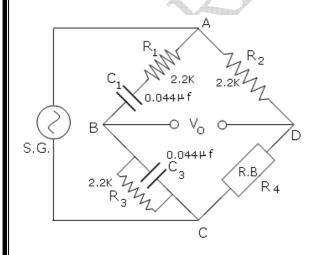
Precautions: -

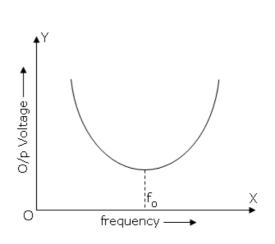
- While measuring the output voltage, the input voltage should be kept at constant value (1V) for each value of frequency.
- 2) The f_0 should be calculated before doing the experiment.

Results: -

Table

S.No.	Frequency (f)	Output voltage (V ₀)
	Hz	V
1.		
2.		
3.		
4.		
	4.7	7
20.		





* * * * *

14. Cathode ray Oscilloscope

(Measurement of peak and rms voltages and frequency of AC)

<u>Aim</u>:- To study the different waveforms, to measure peak and rms voltages and the frequency of A.C.

Apparatus:- A C.R.O and a signal generator.

<u>Theory</u>:- Cathode ray oscilloscope is one of the most useful electronic equipment, which gives a visual representation of electrical quantities, such as voltage and current waveforms in an electrical circuit. It utilizes the properties of cathode rays of being deflected by an electric and magnetic fields and of producing scintillations on a fluorescent screen. Since the inertia of cathode rays is very small, they are able to follow the alterations of very high frequency fields and thus electron beam serves as a practically inertia less pointer. When a varying potential difference is established across two plates between which the beam is passing, it is deflected and moves in accordance with the variation of potential difference. When this electron beam impinges upon a fluorescent screen, a bright luminous spot is produced there which shows and follows faithfully the variation of potential difference.

When an AC voltage is applied to Y-plates, the spot of light moves on the screen vertically up and down in straight line. This line does not reveal the nature of applied voltage waveform. Thus to obtain the actual waveform, a time-base circuit is necessary. A time-base circuit is a circuit which generates a saw-tooth waveform. It causes the spot to move in the horizontal and vertical direction linearly with time. When the vertical motion of the spot produced by the Y-plates due to alternating voltage, is superimposed over the horizontal sweep produced by X-plates, the actual waveform is traced on the screen.

Procedure:- Study of waveforms: To study the waveforms of an A.C voltage, it is led to the y – plates and the time base voltage is given to the X-plates. The size of the figure displayed on the screen, can be adjusted suitably by adjusting the gain controls. The time base frequency can be changed, so as to accommodate one, two or more cycles of the signal. There is a provision in C.R.O to obtain a sine wave or a square wave or a triangular wave.

<u>Measurement of D.C.Voltage</u>: - Deflection on a CRO screen is directly proportional to the voltage applied to the deflecting plates. Therefore, if the screen is first calibrated in terms of known voltage. i.e. the deflection sensitivity is determined, the direct voltage can be

measured by applying it between a pair of deflecting plates. The amount of deflection so produced multiplied by the deflection sensitivity, gives the value of direct voltage.

Measurement of A.C voltage : - To measure the alternating voltage of sinusoidal waveform, The A.C. signal, from the signal generator, is applied across the y – plates. The voltage(deflection) sensitivity band switch (Y-plates) and time base band switch (X-plates) are adjusted such that a steady picture of the waveform is obtained on the screen. The vertical height (l) i.e. peak-to-peak height is measured. When this peak-to-peak height (l) is multiplied by the voltage(deflection) sensitivity (n) i.e. volt/div, we get the peak-to-peak voltage ($2V_o$). From this we get the peak voltage (V_o). The rms voltage V_{rms} is equal to V_o / $\sqrt{2}$. This rms voltage V_{rms} is verified with rms voltage value, measured by the multi-meter.

<u>Measurement of frequency</u>: - An unknown frequency source (signal generator) is connected to y- plates of C.R.O. Time base signal is connected to x – plates(internally connected). We get a sinusoidal wave on the screen, after the adjustment of voltage sensitivity band switch (Y-plates) and time base band switch (X-plates). The horizontal length(l) between two successive peaks is noted. When this horizontal length (l) is multiplied by the time base(m) i.e. \sec/div , we get the time-period(T). The reciprocal of the time-period(1/T) gives the frequency(f). This can be verified with the frequency, measured by the multi-meter.

Precautions:

- 1) The continuity of the connecting wires should be tested first.
- 2) The frequency of the signal generator should be varied such that steady wave form is formed.

Results : -			

Table-1

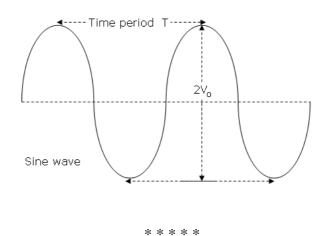
Voltage measurement:

S.No	Peak to peak (Vertical) length. (Divisions) (1)	Voltage Sensitivity. (Volt/Div) (n)	Peak to peak Voltage 2V ₀ =nxl (volts)	Peak voltage V _o =(2V _o /2) (volts)	Rms Voltage $V_{rms}=(V_o J)$ $\sqrt{2}$ (volts)	Measured voltage with Multi-meter (volts)
1.						
2.					4	42
3.						
4.					4	
5.						7

Table -2

Frequency measurement:

S.No.	Peak to peak (Horizontal) length (Divisions) (l)	Time-base Sec/Div (m)	Time-period $T = mxl$ Sec.	Measured frequency f = 1/T Hz	Applied Frequency Hz
1.					
2.	_				
3.					
4.		7			
5.					
6.					



 $^{\rm age}45$

(Measurement of phase difference)

<u>Aim</u>:- To measure the phase difference between the resultant voltage and the current through an R-C circuit.

Apparatus: - Signal generator, CRO, capacitor, variable resistor and connecting terminals.

<u>Formulae</u>:- 1) Theoretical phase difference $\Phi_1 = Tan^{-1} \left(\frac{1}{\omega C R} \right)$

C = Capacitance of the capacitor (μF)

 $R = Resistance of the resistor (\Omega)$

 $\omega = 2\pi f$ Rad/sec.

Where f = The frequency applied (Hz)

2) Practical phase difference $\Phi_2 = Sin^{-1} (\frac{A}{B})$

A = Vertical deflection, at t = 0

B = Maximum vertical deflection.

Theory:- When an AC current is sent through an R-C circuit, the current direction is same in both the elements, R and C. But the voltage directions are different. The voltage across the resistor is in the direction of current and the voltage across the condenser lags behind the current by 90° . Because of this, the resultant voltage also lags behind the current by some angle (Φ) called phase difference. Since the current can't be measured directly by a CRO, the voltage across the resistor is given to CRO, which represents the current direction. So the phase difference is the angle between the voltage across the resistor and the resultant voltage.

Description: The elements, resistor and capacitor of known values are connected in series to the signal generator as shown in the circuit. The first terminal of the capacitor is connected to one of the X- plates and the second terminal of the capacitor is connected to one of the Y-plates. The second plates of X and Y are grounded. This means that the voltage across the resistor is given to Y-plates and the total or resultant voltage across resistor and capacitor is given to X-plates. These two voltages have same frequency. If the voltage values or amplitudes are different and frequencies are same, the superposition of the two waves gives an ellipse, on the CRO screen. The orientation of the ellipse varies as the phase difference varies. As per the formula–1, the phase difference can be changed by changing any one of the three quantities, R, C and f. But for convenience sake the frequency is changed.

Procedure:- The connections are made as shown in the circuit and as said in the description. The time base (X-plates) band switch is kept in external mode. The gain band switch of Y-plates is kept in desired range, so as to get complete maximum size ellipse on the screen. The maximum deflection (B) from the mean position and the deflection (A) at t=0, from the mean position are measured using the divisions on the screen. The experiment is repeated by varying the frequency (f) of the signal generator in equal steps. The values of f, A and B are noted in the table. The values of resistance and capacitance are also noted.

Precautions:-

- 1) The size of the ellipse should be maximum, to minimize the error of measurement.
- 2) The time base (X-plates) band switch should be kept in external mode.

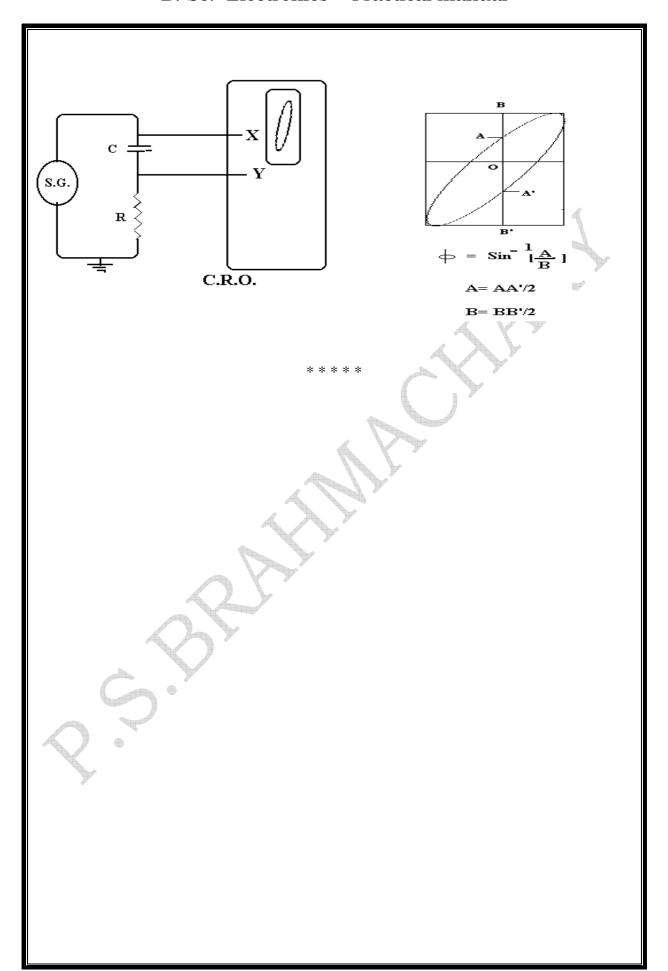
Results :- The calculated value of Φ_1 and Φ_2 are equal.

Table

Resistance (R) = Ω

Capacitance (C) = μF

S.No.	Applied Frequency f (Hz)	Angular Frequency $\omega = 2\pi \text{ f}$ (Rad/sec)	Theoretical Phase $\Phi_1 = Tan^{-1} \left(\frac{1}{\omega C R} \right)$	A (mm)	B (mm)	Practical Phase $\Phi_2 = Sin^{-1} \left(\frac{A}{B}\right)$
1.	G					
2.						
3.						
4.						
5.						
6.						



 $_{
m Page}46$

16. Frequency response of R-L circuit

(Low-pass filter circuit)

 $\underline{\mathbf{Aim}}$: - To observe the frequency response of an R – L circuit, which behaves as a low pass filter circuit and to find the upper 3-db (cut-off) frequency.

<u>Apparatus</u>: - Signal generator, AC milli – voltmeter, connecting terminals, carbon resistors and induction coils (inductors).

Formula: The upper 3-db(cut-off) frequency $f = R / 2\pi L$ Hz.

Where R = Resistance in the circuit (Ω)

L = Inductance in the circuit (H)

Voltage gain
$$G = \frac{e_0}{e_i}$$

 e_o = Out put voltage (V)

 $e_i = In put voltage (V)$

Description and theory:- This R-L filter circuit passes low frequency a.c. readily. The resistance of the resistor is independent of the applied AC frequency. But in case of inductor, as the frequency increases, the reactance ($X_L = \omega L = 2\pi f L$) of the inductor increases. At low frequencies, as the reactance is very low, the inductor acts as short circuit. So at this lower frequencies as $X_L << R$, the P.D. across the inductor is also low compared to that across the resistor, even though the current is high. The total in put voltage (e_i) is equal to the sum of voltages across the inductor and resistor in the R-L circuit. As the voltage across the inductor is so small, the total input (e_i) component appears at the out put(e_0) i.e. across the resistor.

As the frequency of the AC signal increases the reactance X_L of the inductor increases and the potential difference across the inductor also increases. The voltage across the resistor or the out put voltage (e_0) decreases. But at very high frequencies i.e. in M Hz, the reactance of the inductor is so high and the inductor virtually open - circuited and no current flows through the circuit or the resistor. So the voltage across the resistor falls to zero or the out put (e_0) is zero. Hence this circuit passes or sends the low frequency signals (voltages) from the in put to the out put and cut – off the high frequency signals in reaching the out put. So this circuit is called low pass circuit or low pass filter circuit.

Procedure: - First the signal generator is directly connected to the a.c.milli-voltmeter, keeping the frequency of S.G. at 1KHz and adjust the amplitude of the signal to 1 V. i.e. the in put voltage is 1V. This in put voltage 1V should be maintained through out the experiment. Now the a.c. milli - voltmeter is disconnected from the signal generator.

Now again connect the circuit as shown in the figure. In this circuit one end of the inductor L is connected to the resistor R and the other end is connected to the signal generator(S.G.). The second terminal of the resistor is connected to the other terminal of the signal generator. The out put (e_0) is measured across the resistor by a.c milli voltmeter.

Now vary the frequency of AC signal generator from 10 Hz and so on, up to MHz by taking at least 5 readings in each range and note down the values of out put voltage (e_0) using AC milli-voltmeter for each frequency f and calculate the gain ($G = e_0/e_i$) for all values of frequencies and note down the gain ratio in the observation table. Also note the 'log f' values.

Note:-

- 1) The values of R and L are so selected such that the cut off frequency lies in the range 1KHz to 20KHz.
- 2) To measure the out put voltage, digital multi-meter should not be used. Because at higher frequencies i.e. above 5 K Hz it shows less values instead of actual values.

<u>Graph</u>: A graph is plotted between frequency f or log f and gain, by taking the frequency or log f on x – axis and gain on y – axis. This is called frequency response curve. The frequency and gain characteristics are as shown in the figure. The frequency corresponding to 0.707 times to the maximum gain (0.707G_{max}) is noted. It is the upper 3-db(cut-off) frequency. This is the frequency up to which the circuit can allow or pass voltage signal to reach the out put.

Precautions:

- 1) The continuity of the connecting wires should be tested first.
- 2) The frequency of the signal generator should varied from the lowest value.
- 3) The in put must be maintained at constant value through out the experiment.

<u>Table</u>

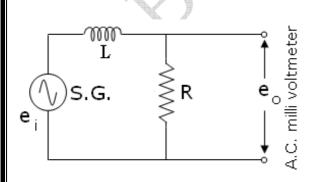
The input voltage $e_i = 1V$

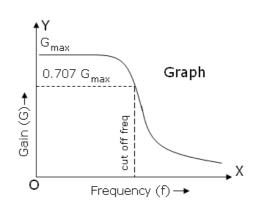
$$R = \Omega$$

$$L =$$

Η

S.No.	Frequency (Hz)	Out put voltage (e ₀) (V)	Voltage gain $G = \frac{e_0}{e_i}$	log f
1.				
20.				





* * * * *

17.Frequency response of R – L circuit

(High-pass filter circuit)

 $\underline{\mathbf{Aim}}$: - To observe the frequency response of an R – L circuit, which behaves as a high pass filter circuit and to find the upper 3-db (cut-off) frequency.

<u>Apparatus</u>: - Signal generator, AC milli – voltmeter, connecting terminals, carbon resistors and induction coils (inductors).

Formula: The lower 3-db(cut-off) frequency $f = R / 2\pi L$ Hz.

Where R = Resistance in the circuit (Ω)

L = Inductance in the circuit (H)

Voltage gain
$$G = \frac{e_0}{e_i}$$

 $e_o = Out put voltage (V)$

 $e_i = In put voltage (V)$

Description and theory: This R-L filter circuit passes high frequency a.c. readily. The resistance of the resistor is independent of the applied AC frequency. But in case of inductor, as the frequency increases, the reactance ($X_L = \omega L = 2\pi f L$) of the inductor increases. At low frequencies, as the reactance is very low, the inductor acts as short circuit and maximum current passes through the circuit. So at this lower frequencies as $X_L << R$, the P.D. across the inductor is also low compared to that across the resistor (IR). The total in put voltage (e_i) is equal to the sum of voltages across the inductor and resistor in the R-L circuit. As the voltage across the inductor or the out put (e_0) is so small and the total input (e_i) component appears across the resistor.

As the frequency of the AC signal increases the reactance X_L of the inductor increases and the current through the circuit decreases. Also potential difference across the resistor decreases. So the voltage across the inductor or the out put voltage (e_0) increases. But at very high frequencies i.e. in M Hz, the reactance of the inductor is so high and the inductor virtually open - circuited and minimum current flows through the circuit or the resistor. So the voltage across the resistor falls to zero and the total input voltage appears across the inductor or at the out put. So the out put (e_0) across the inductor is maximum. Hence this circuit passes or sends the high frequency signals (voltages) from the in put to the out put and cut – off the low frequency signals in reaching the out put. So this circuit is called high pass circuit or high pass filter circuit.

Procedure: - First the signal generator is directly connected to the a.c.milli-voltmeter, keeping the frequency of S.G. at 1KHz and adjust the amplitude of the signal to 1 V. i.e. the in put voltage is 1V. This in put voltage 1V should be maintained through out the experiment. Now the a.c. milli - voltmeter is disconnected from the signal generator.

Now again connect the circuit as shown in the figure. In this circuit one end of the resistor R is connected to the inductor L and the other end is connected to the signal generator(S.G.). The second terminal of the inductor is connected to the other terminal of the signal generator. The out put (e_0) is measured across the inductor L by a.c milli voltmeter.

Now vary the frequency of AC signal generator from 10 Hz and so on, up to MHz by taking at least 5 readings in each range and note down the values of out put voltage (e_0) using AC milli-voltmeter for each frequency f and calculate the gain ($G = e_0/e_i$) for all values of frequencies and note down the gain ratio in the observation table. Also note the 'log f' values.

Note:-

- 1) The values of R and L are so selected such that the cut off frequency lies in the range 1KHz to 20KHz.
- 2) To measure the out put voltage, digital multi-meter should not be used. Because at higher frequencies i.e. above 5 K Hz it shows less values instead of actual values.

<u>Graph</u>: A graph is plotted between frequency f or log f and gain, by taking the frequency or log f on x – axis and gain on y – axis. This is called frequency response curve. The frequency and gain characteristics are as shown in the figure. The frequency corresponding to 0.707 times to the maximum gain (0.707G_{max}) is noted. It is the lower 3-db(cut-off) frequency. This is the frequency above which the circuit can allow or pass voltage signal to reach the out put.

Precautions:

- 1) The continuity of the connecting wires should be tested first.
- 2) The frequency of the signal generator should varied from the lowest value.
- 3) The in put must be maintained at constant value through out the experiment.

<u>Table</u>

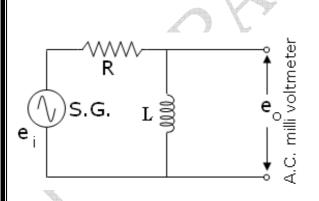
The input voltage $e_i = 1V$

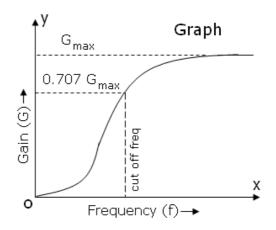
 $R = \Omega$

L =

Η

				A /
S.No.	Frequency (Hz)	Out put voltage (e ₀) (V)	Voltage gain $G = \frac{e_0}{e_i}$	Log f
1.				7
				9
			AVT	
20.				





* * * * *

18. P - N Junction diode

<u>Aim</u>: To study the Volt- ampere (V-I) characteristics of a junction diode, both in forward bias and reverse bias. And also to find out the following physical quantities.

- 1. knee voltage or cut-in voltage or threshold voltage (V_o).
- 2. Static or dc forward resistance (R_{dc}).
- 3. Dynamic or ac forward resistance (R_{ac}).
- 4. Reverse saturation current (I_0) .
- 5. Reverse static resistance (R_r) .

Apparatus: - Junction diode, battery (0-10 V), rheostat, plug key, dc voltmeter (0-10V), milli-ammeter (0-100mA) and micro-ammeter (0-200μA).

<u>Formula</u>:- 1. Static or dc forward resistance $R_{dc} = \frac{V_f}{I_f} \Omega$

Where $V_f = Forward voltage (V) = OB$

 I_f = Forward current (mA) = OE

2. Dynamic or ac forward resistance $R_{ac} = \frac{\Delta V_f}{\Delta I_f}$ Ω

Where ΔV_f = Change in the forward voltage (V) = AC

 ΔI_f = change in the forward current (mA) = DF

3. Reverse static resistance $R_r = \frac{V_r}{I_r}$ Ω

Where $V_r = \text{Reverse voltage } (V) = \text{OG}$

 I_r = Reverse current (mA) = OH

Theory: A P-N junction is formed from a piece of a semi-conductor (Ge or Si) by diffusing third group material to one half and fifth group material to the other half. The first half becomes P-type and the second half becomes N-type. The plane dividing the two is known as P-N junction. The P-region has holes and N-region has electrons as majority charge carriers. Also, a few electrons are present in P-region and a few holes in N-region as minority charge carriers.

The majority charge carriers near the junction cross over the junction to the other side and combine with the opposite charge carriers and become neutral. This region is called depletion region or space charge region. This region lies on the two sides of the junction. In the depletion region, on P-side immobile negative ions and on N-side immobile positive ions lie, with no charge carriers. This gives rise a potential called potential barrier (V_B) , which prevents respective majority charge carriers from crossing the barrier region. As the reverse bias increases the width of the depletion increases and the barrier potential (V_B) also increases. In the forward bias the V_B value decreases.

Procedure:- In the <u>forward bias</u> the battery positive terminal is connected to p-region and negative terminal is connected to N-region. The connections are made as shown in the figure-1. The voltmeter is connected across the diode to measure the voltage applied, the milli-ammeter is connected in series to the diode, to measure the current flowing through the diode. The voltage applied is increased in steps of 0.1 V or 0.2 V, starting from zero, the corresponding current from the milli-ammeter is noted in the table-1.

<u>Graph-1</u>: A graph is drawn, in the 1st quadrant, by taking voltage on X-axis and current on Y-axis. From the graph the threshold voltage V_o is noted. The values V_f , I_f , and ΔV_f , ΔI_f are also noted as shown in the graph, to measure the static and dynamic resistances respectively.

In the <u>reverse bias</u> the battery positive terminal is connected to N-region and negative terminal is connected to P-region. The connections are made as shown in the figure-2. The voltmeter is connected across the diode to measure the voltage applied, the micro-ammeter is connected in series to the diode, to measure the current flowing through the diode. The voltage applied is increased in steps of 1 V or 2 V, starting from zero, the corresponding current from the micro-ammeter is noted in the table-2.

<u>Graph-2</u>:- A graph is drawn, in the 3^{rd} quadrant, by taking voltage on negative X-axis and current on negative Y-axis. Here, in the 3^{rd} quadrant, deferent scale may be taken for convenience. From the graph the reverse saturation current I_o is noted. The values V_r , I_r , are also noted as shown in the graph, to measure the reverse static resistance.

Precautions:-

- 1) For silicon diode the applied voltage should be more than for Germanium diode.
- 2) Very high voltages should not be applied in reverse bias which cause damage to the diode.

Results:-

Table -1

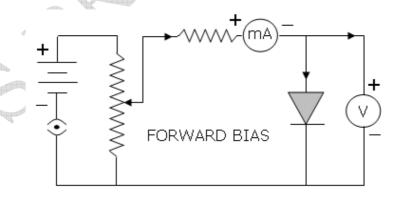
Forward bias

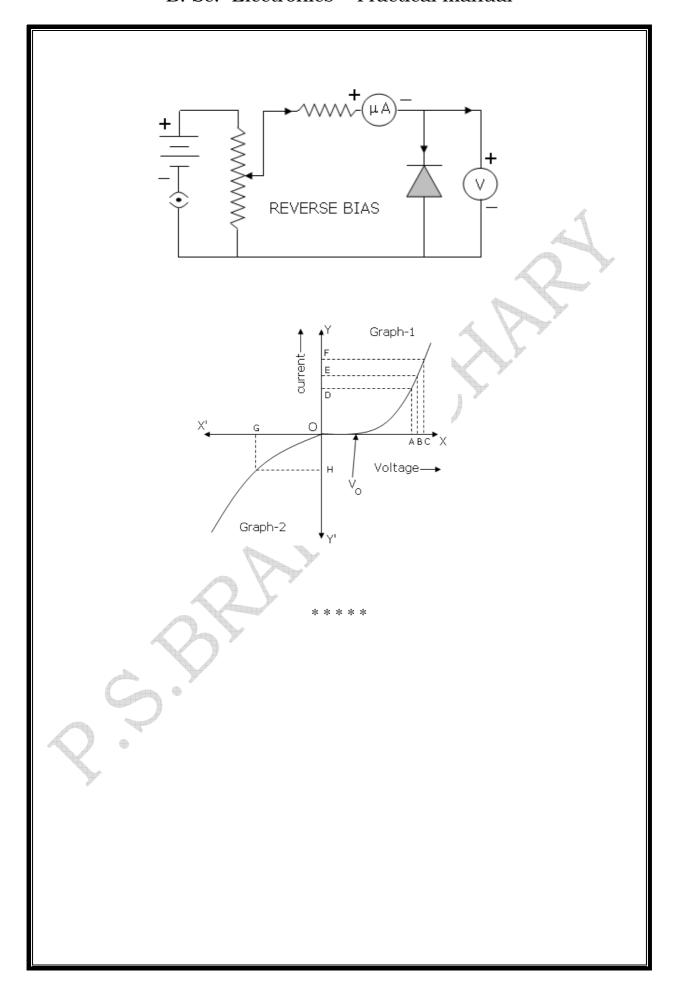
	Applied	Current
S.No.	Voltage	Through diode
	V_f (V)	I_f (mA)
1.		
2.		
3.		
4.		
5.		
6.		
7.		
8.		4
9.		4
10.		

<u>Table – 2</u>

R	everse	hias
- 17	CVCISC	mas

	Applied	Current
S.No.	Voltage	Through diode
	V_r (V)	I_r (μA)
1.		
2.		
3.		*
4.		
5.		
6.		
7.		
8.		
9.		
10.		





 $^{\text{age}}$

19. Zener diode

<u>Aim</u>: To study the Volt- ampere (V-I) characteristics of a Zener diode, both in forward bias and reverse bias. And also to find out the following physical quantities.

- 1. knee voltage or cut-in voltage or threshold voltage (V_o) in forward bias.
- 2. Dynamic or ac forward resistance (R_Z).
- 3. The Zener break down voltage in reverse bias (V_z)

Apparatus: - Zener diode, battery (0-10 V), rheostat, plug key, dc voltmeter (0-10V), milliammeter (0-100mA) and micro-ammeter (0-500μA).

Formula: Dynamic or ac forward resistance $R_Z = \frac{\Delta V_f}{\Delta I_f} \Omega$

Where ΔV_f = Change in the forward voltage (V) = AC

 ΔI_f = change in the forward current (mA) = DF

Theory: The Zener diode is an ordinary P-N junction diode (generally Silicon is preferable), except that it is properly doped to have a very sharp and almost vertical break down. This is exclusively operated under reverse bias conditions and designed to operate in break down region with out damage. As this is a heavily doped diode, the depletion region is very narrow (150-200A°). When the reverse bias across the diode is increased, the electric field becomes intense (in the order of 10⁸ V/m) and all the covalent bonds break at a time, (minority charge carriers come from valance band to conduction bond) which is called Zener break down. Then a large number of electron-hole pairs production occur. This results a sharp increase in the reverse current.

<u>Procedure</u>:- In the <u>forward bias</u> the battery positive terminal is connected to p-region and negative terminal is connected to N-region. The connections are made as shown in the figure-1. The voltmeter is connected across the Zener diode to measure the voltage applied, the milli-ammeter is connected in series to the diode, to measure the current flowing through the diode. The voltage applied is increased in steps of 0.1 V, starting from zero, the corresponding current from the milli-ammeter is noted in the table-1.

<u>Graph-1</u>:- A graph is drawn, in the 1st quadrant, by taking voltage on X-axis and current on Y-axis. From the graph the threshold voltage, V_o is noted. The values ΔV_f and ΔI_f are noted as shown in the graph, to measure the dynamic resistance, R_z of the Zener diode.

In the <u>reverse bias</u> the battery positive terminal is connected to N-region and negative terminal is connected to P-region. The connections are made as shown in the figure-2. The voltmeter is connected across the diode to measure the voltage applied, the micro-ammeter is connected in series to the diode, to measure the current flowing through the diode. The voltage applied is increased in steps of 1 V, starting from zero, until the Zener break down occurs, the corresponding current from the micro-ammeter is noted in the table-2.

<u>Graph-2</u>:- A graph is drawn, in the 3^{rd} quadrant, by taking voltage on negative X-axis and current on negative Y-axis. Here, in the 3^{rd} quadrant, deferent scale may be taken for convenience. From the graph the Zener break down voltage, V_z is noted.

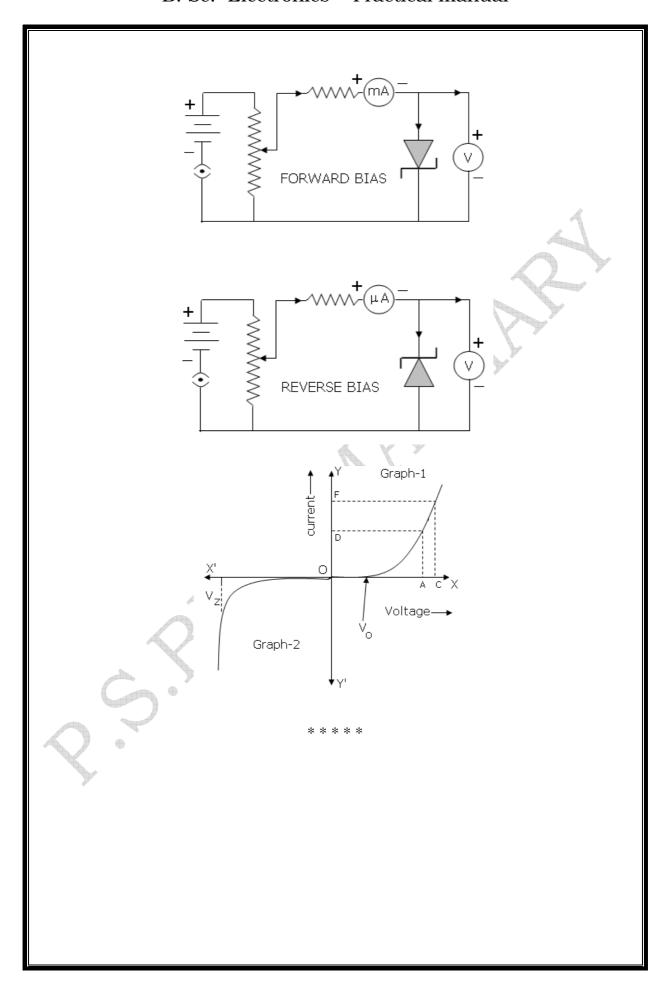
Precautions:

- 1) Check the polarities of Zener diode before making connections.
- 2) The connections should be tight.
- 3) 3. The power supply should be 'on' only when the observations are taken.

Results :-	
<u> Table –1</u>	Table – 2
Forward bias	Reverse bias

	S.No.	Applied	Current
		Voltage	Through diode
		V_f (V)	I_f (mA)
	1.		
	2.		
4	3.		
	4.	-	
	5.		
	6.		
	7.		
	8.		
	9.		
	10.		

S.No.	Applied	Current		
	Voltage	Through diode		
	$V_r(V)$	I_r (μA)		
1.				
2.				
3.				
4.				
5.				
6.				
7.				
8.				
9.				
10.				



 $^{\rm age}61$

20. Rectifiers and filters

<u>Aim</u>: - To construct a DC power supply and to find the percentage of ripple-factor and percentage of regulation.

<u>Apparatus</u>:- Transformer 230V/15V (step-down), four IN 4007 diodes, two 470μF/25V electrolytic capacitors (C_1 , C_2), one Polycarbonate condenser (C_3), 45mH inductor, $1K\Omega$ resistance pot, digital multi-meter, 0 -100 mA range milli-ammeter, three keys (K_1 , K_2 , K_3),and connecting terminals.

Formulae: - 1) Percentage of ripple – factor
$$\gamma = \frac{V_{ac}}{V_{dc}} x 100$$

Where $V_{ac} = r.m.s.$ value of a.c. component (superimposed on DC) (volt)

 V_{dc} = Value of d.c. component (volt)

2) Percentage of regulation
$$R = \frac{V_{NL} - V_{FL}}{V_{FL}} X100$$

Where $V_{NL} = d.c.$ voltage with <u>no load</u> (volt)

 $V_{FL} = d.c.$ voltage with <u>load</u> (volt)

<u>Theory</u>: - The DC power – supply consists of 4 parts. 1) Transformer 2) Rectifier 3) Filter 4) Voltage regulator.

<u>Transformer</u>'s job is to step-up or to step-down the AC supply voltage as per our requirement. <u>Rectifier</u> is the circuit with one or more diodes to convert a.c. voltage into pulsating d.c. voltage. <u>Filter</u> is the circuit that removes the pulsations or ripples present in the out put of the rectifier. <u>Voltage regulator</u> keeps the terminal voltage of the d.c. power supply constant, even if the a.c. input to the transformer varies or the load varies. (In the present experiment the percentage of voltage regulation is calculated without using the voltage regulator circuit.)

<u>Step 1</u>:- The out-put (secondary coil) of the transformer should be given to the in – put of the rectifier at the terminals 1 and 2.

Rectifiers – Rectifiers are of three types

1) <u>Half- wave rectifier</u>:- This consists of only one diode, as shown in fig 1. In the half-wave rectification, during the positive half-cycle of the ac in-put (Fig 4a), the diode is for-ward biased and it conducts current. During negative half-cycle, the diode is

reverse biased and it does not conduct the current. So, in this rectifier only half of the wave is rectified. The out-put dc voltage, across the terminals A and B (with the load) is as in fig 4b. Its maximum efficiency is 40.6%.

- 2) Centre-tap full-wave rectifier: In this full-wave rectifier two diodes D_1 and D_2 are connected from terminals 1 and 2. The other terminals of D_1 and D_2 are connected to a common terminal (A). The centre tap of the transformer is taken as ground (B), as shown in fig 2. When the in put ac is switched on, during the positive half-cycle, the terminal 1 becomes positive and D_1 is for-ward biased and it conducts current, terminal 2 becomes negative and D_2 is reverse biased and it does not conduct. During the negative half-cycle, the terminal 2 becomes positive and D_2 is for-ward biased and it conducts current, terminal 1 becomes negative and D_1 does not conduct. Therefore the two diodes work alternately. The current flow is from A to B (in the load) in both the half cycles and the complete wave is rectified. The out-put dc voltage, across the terminals A and B (with a load) is as in fig 4c. Its maximum efficiency is 81.2 %.
- 3) Bridge-type full-wave rectifier: It is the most frequently used circuit in electronic dc power supplies. In this rectifier, four diodes (D₁, D₂, D₃ and D₄) are connected as a bridge, as shown in the fig 3. The terminals 1 and 2 of the transformer secondary, are connected to the terminals C and D of the bridge, respectively. When the in put ac is switched on, during the positive half-cycle, the terminal 1 becomes positive, terminal 2 becomes negative. So D₁ and D₃ are for-ward biased and they conduct current, and D₂ and D₄ are reverse biased and they do not conduct. During the negative half-cycle, the terminal 2 becomes positive, terminal 1 becomes negative and D₂ and D₄ are forward biased and they conduct current, and D₁ and D₃ are reverse biased and they do not conduct. Therefore the two pairs of diodes work alternately. So the complete wave is rectified. The current flow is from A to B (in the load) in both the half cycles. The out-put dc voltage measured, across the terminals A and B (with load), is as in fig 4c. Its maximum efficiency is 81.2 %.

Step 2:- The out-put of the rectifier should be given to the filter as in – put i.e. the terminals \underline{A} and \underline{B} should be connected to the terminals \underline{A}^I and \underline{B}^I , respectively. The load ($\underline{R}_{\underline{L}}$) is connected after the filter circuit.

<u>Filters</u> - The most commonly used filter circuits are 1) Shunt capacitor filter 2) Series inductor filter 3) Choke in put filter or L- filter and 4) Capacitor in put filter or π -filter.

- 1. Shunt capacitor filter: The shunt capacitor filter is obtained by placing a capacitor C_2 in parallel with a load resistor R_L . The capacitor C_2 is so chosen that its reactance ($1/\omega C_2$) at the frequency of a.c. main, is very small as compared to the load R_L . Then the a.c components find a low reactance shunt path through the capacitor and are mostly bypassed. Thus, the a.c components or ripples flowing through the load decrease or in other words ripples are filtered from the output voltage.
- 2. Series inductor filter: The series inductor filter is obtained by placing an inductor coil (L) in series with a load resistor R_L. The inductor stores energy as magnetic energy, when the current is above its average value and delivers that energy to the circuit when the current tends to fall below the average level. Thus, it reduces the pulsation of the rectifier output.
- 3. $\underline{L-filter}$: To meet the demand for the lower ripple factors, series inductor and shunt capacitor are combined together to give L-filter. In this filter the series inductor passes the d.c components from the rectifier output but introduces the high reactance (ωL) path for a.c . The a.c components that remain after passing through the inductor are bypassed by the shunt capacitor C_2 which offers a low reactance ($1/\omega C_2$) to them, but infinite resistance to d.c . Thus the output across the load R_L possesses less a.c. component or the low ripple factor.
- 4. $\underline{\pi}$ filter: When higher output voltage at light loads is desired, an input capacitor C_1 is added to L filter to form a π -filter. The use of π filter provides an output voltage that approaches the peak value of the a.c potential of the source, the ripple components being very small.

About keys in the filter circuit: -If K_1 or K_3 is in closed position the current flows through the concern capacitor and it works. If the key is in open position the concern capacitor does not work. Regarding the key K_2 , the case is quite different. If K_2 is opened the current flows

through the inductor and it works. If this key is closed, the current flows through the key, but not through the inductor, as the inductor offers some reactance. So the inductor does not work, if the key K_2 is closed.

- 1. Shunt capacitor filter: K_1 should be in open position. K_2 and K_3 should be in closed position.
- 2. Series inductor filter: K_1 , K_2 and K_3 should be in open position.
- 3. Choke in put filter or L- filter: K_1 and K_2 should be in open position and K_3 should be in closed position.
- 4. <u>Capacitor in put filter or π -filter: K_2 should be in open position. K_1 and K_3 should be in closed position.</u>

Procedure: - The out-put ac signal from the secondary (terminals 1 and 2)of the transformer is given, as in put, to any **one** of the **desired** rectifier as said above. Generally we will take the full-wave rectifier (centre tap-type or bridge-type) to get maximum efficiency. The out put of the rectifier (terminals A and B) is given to the filter circuit (terminals A^I and B^I), as in put. Select **one** of the filter. The load R_L , in series with a milli-ammeter, is connected after the filter circuit. To measure the remaining ac component after filtration, a capacitor C_3 is connected at the end as shown in the fig 5.

Adjust the load current I_L to 20 mA by adjusting the load resistance R_L . Measure V_{dc} and V_{ac} across EG and FG respectively, using digital multi meter by keeping the band switch in proper , dc voltage and ac voltage, positions. Increase the load current in steps of 20 mA up to 100 mA and measure the corresponding V_{dc} and V_{ac} values. Note the I_L , V_{dc} and V_{ac} values in the table and calculate the corresponding ripple-factor percentages as per the formula-1

<u>Graph</u>: - A graph is drawn by taking Load current I_L on X- axis and V_{dc} on Y-axis, it gives a straight line or a slight curve 'PQ'. The V_{dc} value decreases as I_L increases. If PQ line is extended back it cuts the Y – axis at a point R. The 'OR' value or the <u>maximum V_{dc} value is called voltage at no load (V_{NL}).</u> All the other V_{dc} values are called voltage at full load (V_{FL}), this means the voltage at that particular load resistance (R_L).

The percentage of regulation (R) is calculated by substituting the V_{NL} and V_{FL} values in the formula-2, for each value of load current (I_L).

The experiment is repeated with other rectifiers and filters also. The tabular form and the formulae1 and 2 are same for any combination of rectifier and filter.

Precautions: -

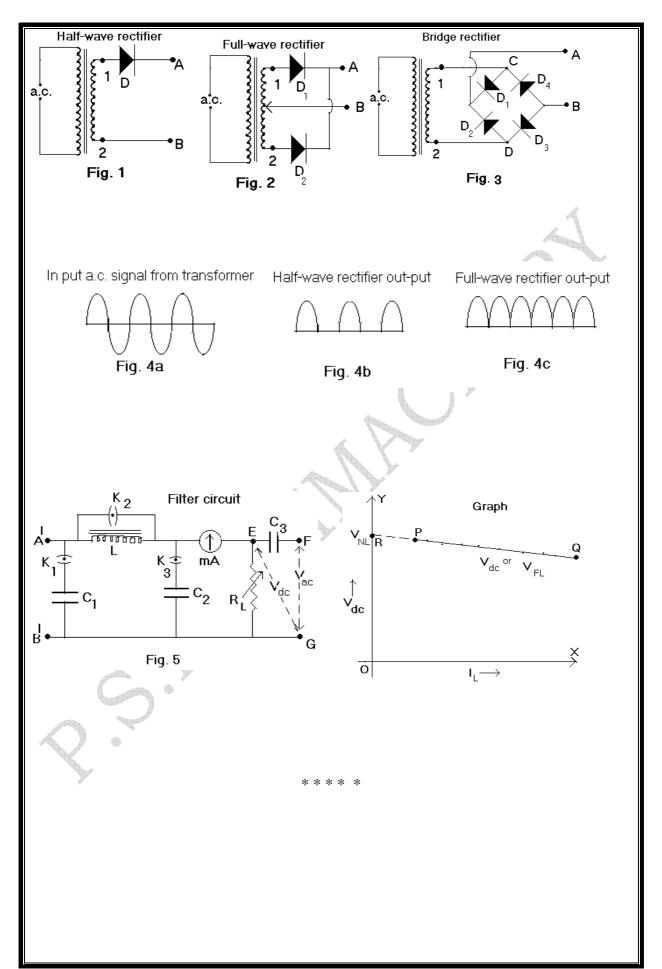
- 1) The keys K_1 , K_2 and K_3 should be kept in proper position as per the selected filter.
- 2) The band switch of the multi-meter should be kept in proper range and position while measuring V_{dc} and V_{ac} values.

 $\underline{Result}: \text{- The percentage of ripple-factor } (\gamma) \text{ and percentage of regulation } (\ R\) \text{ increase with }$ increase of load current ($I_L)$

Table

Voltage with no load $V_{NL} = V$

		ANY Value	iii .		
S.No.	Load current (I _L) mA	V_{dc} or V_{FL} (V)	V _{ac} (V)	% of ripple-factor $\gamma = \frac{V_{ac}}{V_{dc}} \times 100$	% of regulation $R = \frac{V_{NL} - V_{FL}}{V_{FL}} X100$
1.					
2.					
3.					
4.					
5.					



 $P_{age}6$

21.Bipolar Junction Transistor

<u>Aim</u>: To draw the in put and out put characteristics of the given n-p-n transistor in common emitter configuration and to find out the values of h-parameters of the transistor.

<u>Apparatus</u>:- Two variable dc power supplies, two voltmeters, one milliammeter, one microammeter, n-p-n transistor and connecting terminals.

Formulae: - From in put characteristics

- 1) In put impedance or resistance $h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} \Omega$ at constant V_{CE}
- 2) Reverse voltage ratio $h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}}$ at constant I_B

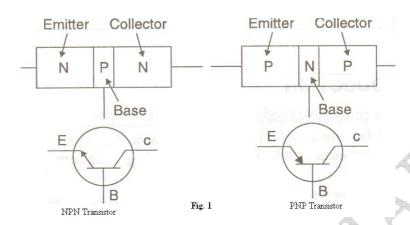
From out put characteristics

- 3) For ward current ratio $h_{fe} = \frac{\Delta I_C}{\Delta I_B}$ at constant V_{CE}
- 4) Out put admittance $h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} \Omega^{-1}$ at constant I_B

THEORY: Bipolar junction transistor (BJT) consists of a silicon (or germanium) crystal in which a thin layer of N - type silicon is sandwiched between two layers of P-type silicon, to form the *P-N-P* junction transistor. A thin layer of P-type lies in between two layers of N - type material to form the N-P-N transistor. The central section is called the base, one of the outer sections the emitter, and the other outer section the collector. The base region, through which injected carriers pass, must be very thin. The two end sections, emitter and collector of the *N-P-N* transistor contain a number of free electrons, while the central section, base, possesses an excess of holes. And vice versa in the *P-N-P* transistor. At each junction, depletion regions develop small barrier potential. These are modified by the external applied voltages.

The basic function of the transistor is amplification. A transistor comprises two p-n junctions. One junction (emitter-base) is forward biased and has a low resistance, the other junction (collector-base) is reverse biased and has a high resistance. A weak signal is introduced in the low resistance circuit and the output is taken from the high resistance circuit, which is reverse biased. Therefore, a transistor transfers a signal from a low resistance

region to high resistance region. The prefix 'trans' means the signal transfer while 'istor' means resistor. Hence the name transistor.



The circuit symbols of N-P-N and P-N-P transistors are shown in Fig.1. The emitter (E) is distinguished from the collector (c) by an arrow which indicates the direction of conventional current flow (opposite to the flow of electrons) with forward bias. In both cases the arrow head is from P to N. Both the emitter and collector touch the base with some inclination.

Description:- A variable dc power supply V_{BB} is connected between the base B and emitter E of the NPN transistor. This applies a for ward bias V_{BE} to the emitter-base junction. To measure V_{BE} , a voltmeter is connected across B and E. To measure the base current I_B a micro-ammeter is connected in series to the base. The emitter E is grounded. Another variable dc power supply V_{CC} is connected between the collector C and emitter E. This applies a reverse bias to the collector-base junction. To measure collector voltage or out put voltage V_{CE} , a voltmeter is connected across C and E. To measure the collector current I_C a milli-ammeter is connected in series to the collector. Here the emitter is common to both the in put and out put

terminals. So this is the "common emitter configuration". $V_{BB} = V_{CC}$ Fig.2

<u>Procedure</u>:-The circuit is connected as shown in Fig. 2. To study the <u>in put characteristics</u>, [The curves showing the variation of the base current I_B with base-emitter voltage V_{BE} at constant collector-emitter voltage V_{CE}] the out put voltage V_{CE} is kept at constant value (0 V – 15 V) and the in put voltage V_{BE} is varied insteps and the corresponding base current I_B is noted in the table-1. The process is repeated for different values of V_{CE} . The input characteristics are shown in <u>Fig. 3</u>.

<u>Graph-1</u>:- A graph is drawn by taking in put voltage V_{BE} on X-axis and in put current I_B on Y-axis by keeping V_{CE} constant. The same graph is drawn for different values of V_{CE} . From these curves we calculate two h-parameters 1) In put impedance(h_{ie}) and 2) Reverse voltage ratio (h_{re}) as shown in the Fig.3.

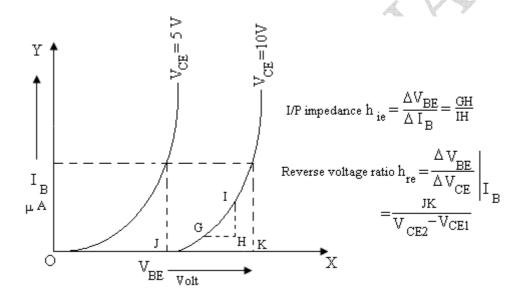


Fig.3

(i) These characteristics resemble to those of a forward biased junction diode because the base-emitter section of transistor is a junction diode and it is forward biased. (ii) The base current increases non-linearly with increase in base voltage.

To study the <u>out put characteristics</u>, [The curves showing the variation of the collector current I_C with collector-emitter voltage V_{CE} at constant base current I_B] the in put current I_B is kept at constant value ($0~\mu A - 100~\mu A$) and the out put voltage V_{CE} is varied insteps and the corresponding collector current I_C is noted in the table-2. The process is repeated for different values of I_B . The out put characteristics are shown in <u>Fig. 4.</u>

<u>Graph-2</u>:- A graph is drawn by taking out put voltage V_{CE} on X-axis and out put current I_C on Y-axis by keeping I_B constant. The same graph is drawn for different values of I_B . From these curves we calculate two more h-parameters 1) Out put admittance (h_{oe}) and 2) For ward current ratio (h_{fe}) as shown in the Fig.4.

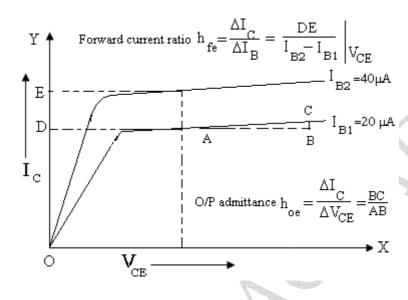


Fig.4

(i)The collector current I_C varies rapidly with V_{CE} for very small voltage (say upto $V_{CE} = 2$ volt). After this collector current becomes almost constant and is decided entirely by base current I_B . It then becomes independent of V_{CE} . (ii) As the base current rises, the effect of collector voltage on the collector current also increases. (iii) The collector current I_C is not zero when base current is zero. This is due to minority charge carriers. (iv) Since the input current I_B is measured in microampere and output current I_C is measured in milliampere, the common emitter configuration exhibits a current amplification.

Precautions:-

- 1) Check the continuity of the connecting terminals before going to connect the circuit.
- 2) Identify the emitter, base and collector of the transistor properly before connecting it in the circuit.
- 3) While taking the readings in the table-2 V_{CE} should also be increased after I_C attaining saturation value.

Results :- 1) In put impedance
$$h_{ie} = \frac{\Delta V_{BE}}{\Delta I_B} = \frac{GH}{IH} =$$

 Ω at constant V_{CE}

2) Reverse voltage ratio
$$h_{re} = \frac{\Delta V_{BE}}{\Delta V_{CE}} = \frac{JK}{V_{CE2} - V_{CE1}} =$$

at constant I_B

3) For ward current ratio
$$h_{fe} = \frac{\Delta I_C}{\Delta I_B} = \frac{DE}{I_{B2} - I_{B1}} =$$
 at constant V_{CE}

4) Out put admittance
$$h_{oe} = \frac{\Delta I_C}{\Delta V_{CE}} = \frac{BC}{AB} = \Omega^{-1}$$
 at constant I_B

Table-1

Table-2

In put characteristics

Out put characteristics

	V _{CE1} =	- V	$V_{CE2} = V$	
0.	V_{BE}	I_B	V_{BE}	I_{B}
S.No.	(Volt)	(µA)	(Volt)	(µA)
				A
				D
			1	

	$I_{B1} =$	(µA)	$I_{B2} =$	(µA)
0.	V_{CE}	I_{C}	V_{CE}	I_{C}
S.No.	(Volt)	(mA)	(Volt)	(mA)

22.Field - Effect Transistor

<u>Aim</u>: To draw and study the out put and transfer characteristics of the given FET and to determine its parameters.

<u>Apparatus</u>:- FET, two variable power supplies, two voltmeters, milliammeter and connecting terminals.

Formulae :-

1) ON resistance of FET, i.e reciprocal of the slope drawn to the <u>out put characteristics</u> <u>curve near the origin.</u> $r_{ON} = \frac{\Delta V_{DS}}{\Delta I_{D}} \Omega$ at constant V_{GS} .

- 2) Drain resistance of FET $r_d = \frac{\Delta V_{DS}}{\Delta I_D} \Omega$ at constant V_{GS} . This slope includes both ohmic and saturation regions.
- 3) Transconductance or mutual conductance i.e. the slope drawn to the <u>transfer</u> characteristics curve

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \Omega^{-1}$$
 at constant V_{DS}.

4) Amplification factor $\mu = r_d \times g_m$.

THEORY: The field effect transistor (FET) is a three terminal semiconductor device in which the current is controlled by an applied electric field. It is also called a 'unipolar transistor' because in it the current is carried by one type of carriers i.e. the majority charge carriers. There are two main categories of field effect transistors. Junction field effect transistor (JFET) is one of them.

The junction field-effect transistor (JFET) consists of a segment of semi-conductor material (either N -type or P-type) resulting in either an N-channel JFET or a P-channel JFET. The basic structure of an N-channel JFET is shown in Fig. 1. Ohmic contacts are made to the two ends of an N-type semiconductor bar and current flows along the length of the bar when a voltage is applied between the two ends. The left end of the bar is called the *source* (S), through which the majority carriers (electrons in this case) enter the channel and the right end is called the *drain* (D) through which the majority carriers leave the bar. On the upper and lower sides of the N-type bar, near to its centre, heavily doped P-type material is made to form by diffusion. These junctions form two P-N diodes and are called the gate (G), which control the carrier flow. The region of N-type material between the two gate regions is called

<u>channel</u> through which the majority carriers move from source to drain. The source, drain, and gate terminals in FET are similar to that of emitter, collector and base terminals, respectively, in case of BJT. The source and drain terminals are interchangeable *i.e.*, either end can be used as source and the other end as drain. The voltage between the gate and source is such that the gate is reverse biased.

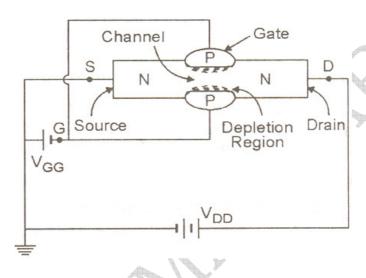


Fig. 1

The P-channel JFET is similar in construction that it uses P-Type bar and two N-type junctions. The majority carriers in this case are holes which flow through the channel.

Schematic symbols for N-channel and P-channel JFETs are shown in Fig.2. The vertical line in the symbol represents the channel to which source S and drain D are connected. The gate arrow always points to N-type material.

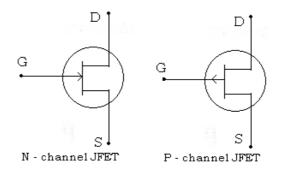


Fig. 2

The application of a voltage V_{DS} (V_{DD} = drain supply voltage) from drain to source will cause the electrons to flow through the channel. The amount of drain current I_D will be determined initially by the value of V_{DS} , since it is just the ohmic resistance of the bar from S to D. Suppose the P-N junctions between gate and source are applied reverse-bias. These two reverse biased P-N junctions develop depletion regions, as shown by the cross-hatching in Fig. 1. The depletion regions are non-conductive. As the reverse bias is increased, the size of the depletion regions increases and the drain current is reduced. When the reverse current is large enough for the two depletion regions to meet, the channel becomes pinched off and the drain current cuts off. The reverse bias required for pinch off is called as pinch off voltage V_p . Thus the drain current through the channel depends upon the degree to which the electric field applied to the channel which decreases the conductance of the transistor. Hence the name 'field-effect transistor (FET)' given to this device.

Description: To study the out put and transfer characteristics the circuit is connected as shown in Fig. 3. Here the FET is n-channel FET. The source S is grounded. The drain D is connected to a voltage source V_{DD} such that it applies a potential V_{DS} between source and drain, to pull the electrons from the source to the drain. The potential V_{DS} and the drain current I_D can be measured from the volt meter and milliammeter connected in the circuit respectively. The gate G is connected to a voltage source V_{GG} such that it applies a reverse bias potential V_{GS} between the gate and source. The potential V_{GS} can be measured from the voltmeter, connected across the gate and source.

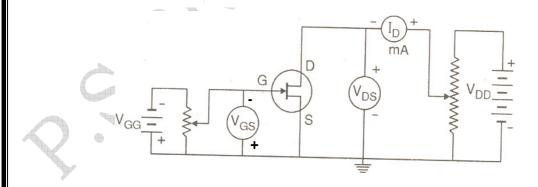
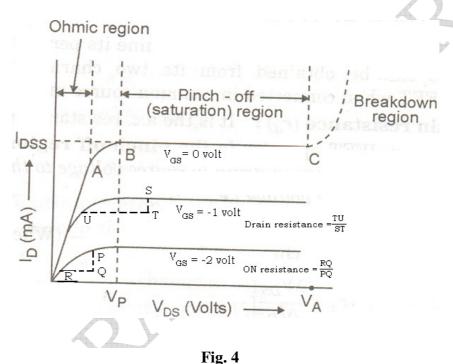


Fig. 3

<u>Procedure</u>:-The circuit is connected as shown in Fig. 3, to study the out put and transfer characteristics.

Output or drain characteristics: Keeping V_{GS} fixed at some value, the drain source voltage (V_{DS}) is changed in steps and corresponding drain current I_D is noted in the table 1. A group of such drain characteristics curves are drawn by setting V_{GS} at a different fixed values (0V, -1V, -2V etc.). Fig. 4 shows out put or drain characteristics.

<u>Graph-1</u>:- A graph is drawn by taking drain voltage V_{DS} on X-axis and drain current I_D on Y-axis by keeping V_{GS} constant. The same graph is drawn for different values of V_{GS} . From these curves we calculate the FET parameters i.e ON resistance (r_{ON}) and drain resistance (r_d) as shown in the Fig.4.



For low values of V_{DS} , drain current I_D varies directly with voltage following Ohm's law. Thus JFET behaves like an ordinary resistor till point A, called knee point, is reached. As V_{DS} further increases, drain current becomes constant at I_{DSS} (maximum drain current). The drain source voltage above which drain current becomes constant is called the pinch off voltage (V_P) and the point B is called pinch off point. The region BC is called saturation region or pinch off region. If V_{DS} is increased beyond avalanche breakdown voltage V_A corresponding to point C, JFET enters the breakdown region where small changes in V_{DS} produce very large changes in I_D . It is due to the avalanche breakdown of reverse-biased gatechannel P-N junction.

<u>Transfer characteristics</u>: It is a plot of 1_D versus V_{GS} for a fixed value of V_{DS} and is shown in Fig. 5. To get the characteristics, V_{DS} is kept fixed while V_{GS} is varied in steps and the corresponding I_D is noted in the table 2.

<u>Graph-2</u>:- A graph is drawn in the 2^{nd} quadrant by taking gate voltage V_{GS} on negative X-axis and drain current I_D on Y-axis by keeping V_{DS} constant. The same graph is drawn for different values of V_{DS} . From these curves we calculate the transconductance of FET(g_m) as shown in the Fig.5. The pinch-off voltage (V_P) can also be known from this graph.

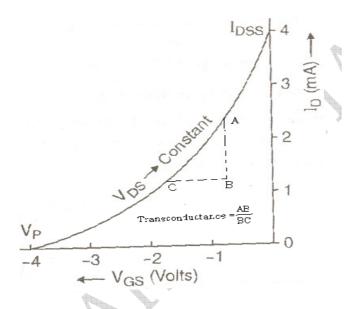


Fig. 5

Precautions:-

- 1) Check the continuity of the connecting terminals before going to connect the circuit.
- 2) Identify the source, drain and gate terminals of the FET properly before connecting it in the circuit.
- 3) While taking the readings in the table-1(for out put characteristics) V_{DS} should also be increased after I_D attaining saturation value.

Results:-

- 1) Short gate drain current I_{DSS} , i.e. saturation drain current for $V_{GS} = 0V$.
 - i. $I_{DSS} = mA$
- 2) Pinch off voltage V_P , i.e. the minimum V_{DS} for saturation drain current. $V_P =$

- 3) ON resistance of FET $r_{ON} = \frac{\Delta V_{DS}}{\Delta I_{D}} = \frac{QR}{PQ} =$
- Ω , at constant V_{GS} .

i.e the reciprocal of the slope drawn to the out put characteristics near the origin.

- 4) Drain resistance of FET $r_d = \frac{\Delta V_{DS}}{\Delta I_D} = \frac{TU}{ST} =$
- Ω at constant $V_{\text{GS}}.$

The reciprocal of the slope includes both ohmic and saturation regions.

5) Transconductance or mutual conductance $g_m = \frac{\Delta I_D}{\Delta V_{GS}} = \frac{AB}{BC} = \frac{\Delta I_D}{\Delta V_{GS}}$

constant $V_{DS.}$

i.e. the slope drawn to the transfer characteristics

6) Amplification factor $\mu = r_d \times g_m =$

Table-2

Out put characteristics

Table-1

Transfer characteristics

	V _{GS1} =	= V	V _{GS2} =	= V
0.	V_{DS}	I_D	V_{DS}	I_D
S.No.	(Volt)	(mA)	(Volt)	(mA)
	Ç		5	

- T	1	$V_{DS1} =$	(V)	$V_{DS2} =$	(V)
Ą	0.	V_{GS}	I_D	V_{GS}	I_D
p	S.No.	(Volt)	(mA)	(Volt)	(mA)

* * * * *

23. Unijunction Transistor (Volt-Ampere Characteristics)

<u>Aim</u>:- To draw the volt-ampere characteristics of the unijunction transistor and to find the UJT pameters.

<u>Apparatus</u>: - UJT, two variable d.c. power supplies, d.c. voltmeter, d.c. milli-ammeter, multi-meter and connecting terminals.

Formulae :-

- 1. Peak point voltage = V_P (V) (From the graph)
- 2. Valley point voltage = V_v (V) (From the graph)

3. Intrinsic stand off ratio
$$\eta = \frac{V_P - V_B}{V_{RR}}$$

Where

 V_B = Barrier potential of P-n junction of Silicon diode = 0.7V V_{BB} = Voltage applied between two bases B_1 and B_2 (V)

4.
$$R_{B1} = \eta R_{BB}$$
 $\therefore \eta = \frac{R_{B1}}{R_{BB}} = \frac{R_{B1}}{R_{B1} + R_{B2}}$

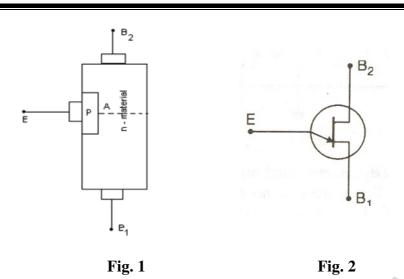
 R_{BB} = Inter base resistance (Ω)

- $5. R_{B2} = R_{BB} R_{B1}$
- 6. Negative resistance = Slope of V-I curve in the negative resistance region.

OR
$$\frac{dV_E}{dI_E} = \frac{AB}{BC}$$

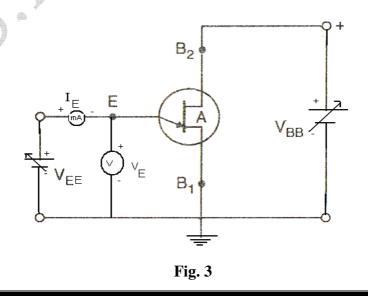
7. Switching efficiency = $V_P - V_V$

Description:- In UJT a Silicon bar is taken and it is lightly doped with V- group material. So the silicon bar acts as lightly doped n – material and on one side of the bar above center a small region is heavily doped with III – group element Which then acts as P – material. Some times instead of doping with 3^{rd} group element a Aluminum wire is made contact at that region and that region acts as P- material. At the two ends of n – type material two wires are connected with ohmic contact, these two terminals are called "Bases" (B_1 - lower and B_2 - upper) and another wire for the P – region is connected and is called "Emitter" (E). The UJT is as shown in Fig. 1



Since the Silicon bar is lightly doped, the resistance between the bases B_2 and B_1 is high and its value ranges from 5 K Ω to 10 K Ω at room temperature. This is called 'double base diode'. If some potential is applied between the bases B_2 and B_1 , a uniform potential gradient is developed between them. Because of its resistance this will also acts as a potential divider and this divides the potential at E. In this UJT it has only one P-n junction, so it is called unijunction transistor. (Since it has three terminals it acts as transistor.)

The <u>circuit symbol of UJT</u> is as shown in the fig. 2. The arrowed terminal is the emitter and it gives the conventional current direction. The emitter arrow is inclined towards the base B_1 terminal because in the '<u>conducting state</u>' the current will flow from emitter to base B_1 .



 $08^{\rm age}$

<u>THEORY</u>:- Case 1:- First the emitter (E) is open i.e. it is given zero potential and a fixed voltage ' V_{BB} ' is applied between two bases B_1 and B_2 , such that B_2 is given positive that is B_2 is at + V_{BB} and B_1 is at zero potential. This V_{BB} produces a current from B_2 to B_1 , which in turn produces a uniform potential gradient between B_2 and B_1 , as the Silicon bar has a resistance of 5 KΩ to 10 KΩ.

The potential at the point 'A' in the Silicon bar, where the emitter region touches the n-type bar is ' ηV_{BB} ', where η is the intrinsic stand off ratio or 'voltage division factor'. The emitter is open means it is given zero potential then the P-n junction is reverse biased, and the current through the junction is zero.

Case 2:- Now a variable voltage V_E from a source V_{EE} is applied between the emitter E and base B_1 When V_E is less than ' ηV_{BB} ' then the P-n junction is reverse biased and the resistance between A and B_1 i.e. R_{B1} is high. In this stage a small reverse leakage current will flow B_2 to E.

When V_E exceeds ηV_{BB} then the junction is for ward biased, but when $V_E \ge \eta V_{BB} + V_B$, holes enter from emitter 'E' to the n-type bar and these are repelled by the base B_2 due to its positive potential and are attracted by B_1 which is at negative potential. (Actually these holes get neutralized by attracting electrons from B_1 , here V_B is the potential barrier of P-n junction). So the conductivity of this part of bar (A to B_1) increases and the resistance R_{B1} decreases. i.e. The emitter current I_E causes a decrease in the resistance which is known as <u>negative resistance characteristic</u>. In this stage emitter voltage V_E also decreases to a low value corresponding to the decrease of resistance R_{B1} . This minimum voltage is called the 'valley point voltage' V_V and the corresponding current is called 'valley point current' I_V . The emitter voltage is maximum when $V_E = \eta V_{BB} + V_B$ and is called 'peak point' voltage (V_P) or 'firing potential'. The current corresponding to V_P is called 'peak point current' I_P . Above I_V the V_E increases gradually and this state is called 'on-state' and the corresponding region in the graph is called 'saturation region'.

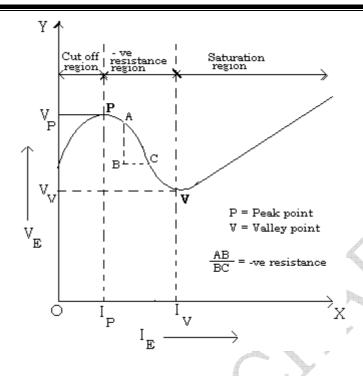


Fig. 4

Procedure: First the emitter is open and the inter base resistance ' R_{BB} ' is measured with a ohmmeter. Now the circuit is connected as shown in Fig.3. Apply a fixed voltage V_{BB} (5V to 10V) between the two bases B_1 and B_2 . Increase the emitter voltage V_E in convenient steps starting from zero. Note the corresponding emitter current I_E . Draw a graph by taking I_E on X-axis and V_E on Y-axis. The shape of the graph is as shown in the Fig. 4. Note the peak point P and valley point V also note the corresponding voltages V_P & V_V and currents I_P & I_V . Find the value of intrinsic stand off ratio η , switching efficiency ($V_P - V_V$), R_{B1} and R_{B2} using the above formulae. Also find the value of the negative resistance of UJT from the slope drawn to the curve in the –ve resistance region.

The characteristic curves can be drawn with different values of V_{BB} . The V_P and V_V values increase with the increasing value of V_{BB} . The I_P and I_V values do not change with the change of V_{BB} . The switching efficiency also increases with increasing value of V_{BB} .

<u>Graph-1</u>:- A graph is drawn by taking emitter current I_E on X-axis and emitter Voltage V_E on Y-axis. From the graph the V_P and V_V values and I_P and I_V values are noted as shown in the graph Fig. 4.

Precautions:-

- 1) The continuity of the connecting terminals should be checked before going to connect the circuit.
- 2) Identify the two bases and emitter of UJT and connect properly.
- 3) The power supply should be 'on' only when the observations are taken.

S. No.	$V_{BB} =$	Volt	$V_{BB} =$	Volt
511101	$I_{E}\left(mA\right)$	V _E (Volt)	$I_{E}\left(mA\right)$	V _E (Volt)

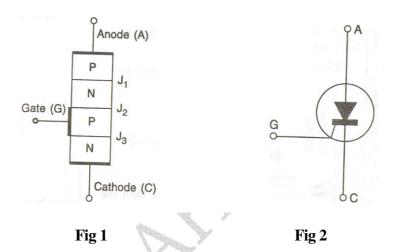
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24. Silicon Controlled Rectifier

<u>Aim</u>:- To draw and study the forward and reverse volt – ampere characteristics of the Silicon Controlled Rectifier.

<u>Apparatus</u>: Silicon Controlled Rectifier, voltmeter, two milli-ammeters, two variable dc.power supplies and connecting terminals.

Theory: When a P-N junction is added to junction transistor, the resulting three junction device is called a silicon controlled rectifier. Thus, the structure of the silicon controlled rectifier (*SCR*) consists of four alternate *P*- and N-type layers, as in the four layer diode. Fig. 1 shows its construction. The circuit symbol for the *SCR* is shown in Fig. 2.



The SCR has three junctions J_1 , J_2 and J_3 and three terminals Anode (A), Cathode (C) and Gate (G). The function of the gate is to control the firing of SCR. In the normal operating conditions of SCR, anode is held at high positive potential with respect to cathode and gate at small positive potential with respect to cathode. Junction areas of SCR are very large since they conduct large currents.

In general the SCR works in two cases 1) When the gate is open 2) when the gate is positive w.r.t. cathode. In both the cases anode is at high positive potential.

<u>Case1</u>:- When the gate is open, no voltage is applied to the gate($I_G = 0$). In this case junctions J_1 and J_3 are in forward bias and junction J_2 is in reverse bias. When the junction J_2 is in reverse bias no current flows through the SCR and it is in cut off state. If the anode voltage V_A is increased at a certain voltage (critical voltage or break over voltage) J_2 breaks down and SCR conducts heavily and is said to be in ON state. Then the anode current I_A increases rapidly. The

maximum anode current that SCR can pass with out destruction is called "holding current, I_H ". Its corresponding voltage is denoted by V_H . If I_A is less than I_H then SCR turns off.

<u>Case 2</u>:- When the gate is positive w.r.t. cathode ($I_G \neq 0$), J_3 is forward biased and J_2 is reverse biased. Then the electrons from N-type material (cathode) across J_3 and move to the gate. Then the gate current starts flowing. So more electrons available at the gate and J_2 breaks and the SCR comes to ON state at the lower voltage of anode. The holding current also decreases with increase of gate current.

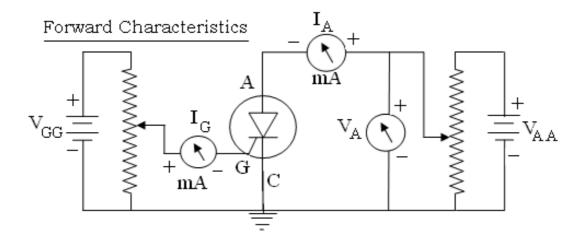


Fig. 3A

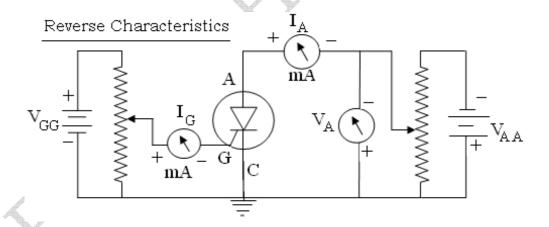


Fig. 3B

Description: To study the for ward volt – ampere characteristics of SCR the circuit is connected as shown in Fig. 3A. Here the Cathode C is grounded. A variable dc voltage source V_{AA} is connected between the anode A and cathode C such that it applies a potential V_A between anode A and cathode C. The anode potential V_A can be measured by the voltmeter connected across the anode and cathode and the anode current I_A can be measured

by the milli-ammeter connected in series to the anode. The gate G is connected to a voltage source V_{GG} such that it supplies a positive gate current I_G . This current is measured by an ammeter which is connected in series to the gate.

To study the reverse characteristics, negative terminal of V_{AA} is connected to the anode A and positive is given to cathode C. The polarities of the voltmeter V_A and milliammeter I_A are interchanged (Fig. 3B). The gate connections are left as it is.

Procedure: First the SCR is connected (Fig. 3A) for forward characteristics. The gate is given zero potential i.e. $I_G = 0$. Now increase the anode voltage V_A in regular intervals and note the values of V_A and corresponding anode current I_A in the table-1. The anode current I_A is so small until the break over voltage ' V_{BO} ' of the anode is reached. At the break over point the current suddenly increases and the voltage falls down and SCR is said to be fired. After the break over point, the voltage and current increase proportionately (Fig.4A). The current corresponding to the point B is called the "holding current". The same procedure is repeated for different values of I_G . It is known that the firing potential and holding current decrease as I_G increases (Fig.4B).

<u>Graph-1</u>:- A graph is drawn, in the 1^{st} quadrant, by taking anode voltage V_A , on X-axis and anode current I_A , on Y-axis. From the graph the break over voltage, V_{BO} is noted. The holding voltage V_H and holding current I_H are also noted at the point B in Fig.4A. The same type graph is drawn for different values of I_G as in Fig.4B.

Now the SCR is connected (Fig. 3B) for reverse characteristics. The negative voltage of the anode V_A , is increased and the corresponding anode current I_A is noted in the table-2. At a particular negative anode voltage the avalanche break down occurs and the anode current suddenly increases. This voltage is called break down voltage. This voltage is noted in the graph as V_{BD} .

<u>Graph-2</u>:- A graph is drawn, in the 3^{rd} quadrant, by taking anode voltage V_A on negative X-axis and anode current I_A on negative Y-axis. Here, in the 3^{rd} quadrant, deferent scale may be taken for convenience. From the graph the break down voltage ' V_{BD} ' is noted.

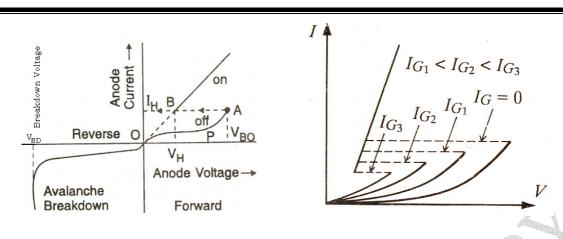


Fig. 4A

Fig. 4B

Precautions:-

- 1) The SCR should not be touched while passing the current through it as the current large.
- 2) SCR comes to ON state by appropriate gate current not by break over voltage.
- 3) SCR should be operated with a minimum value of gate current.

Results:-

Table – 1

Table - 2

For ward characteristics

Reverse characteristics

			4000	W X		
	$I_{G1} =$	mA	$I_{G2} =$	mA	$I_{G3} =$	mA
S.No.	V_{A}	I_A	V_{A}	I_A	V_{A}	I_A
	(Volt)	(mA)	(Volt)	(mA)	(Volt)	(mA)
3	4.					

S.No.	V _A (Volt)	I _A (mA)

25. Unijunction Transistor

(Relaxation Oscillator)

<u>Aim</u>:- To construct a relaxation oscillator using UJT, to measure the frequency of oscillation and comparing it with the theoretical value.

<u>Apparatus</u>: - UJT, resistance box, decade condenser box, variable d.c. power supply, C.R.O. and connecting terminals.

Formula:- Frequency of oscillator
$$f = \frac{1}{2.303RC \log_{10}(\frac{1}{1-\eta})} Hz$$

Where $R = Resistance of the resistor (\Omega)$

C = Capacity of the condenser (F)

 η = Intrinsic stand off ratio = 0.6

Description:- A variable d.c. power supply V_{BB} is connected across the two bases of the UJT Such that B_2 is positive and B_1 is negative. A resistance box 'R' is connected between the base B_2 and emitter 'E'. A. decade condenser box 'C' is connected between the emitter E and base B_1 of the UJT. To measure the voltage across the condenser its two terminals are connected to the Y-plates of the CRO. Here V_{BB} , R and C will form a RC circuit incase of charging or growth of the condenser. But the condenser discharges or decays through the R_{B1} when the UJT comes to conducting state. The resultant voltage wave form is observed on the screen of the CRO.

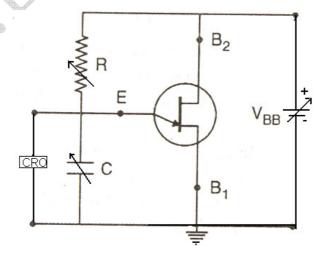


Fig. 1

THEORY:- The UJT has negative resistance characteristic, because of this character the UJT provides trigger pulse. Any one of the three terminals can be taken for triggering pulse. The UJT can be used as relaxation oscillator i.e. it produces non-sinusoidal waves. The circuit diagram of relaxation oscillator is as shown in fig. 1.

First the capacitor 'C' starts charging through the resistor R when V_{BB} is switched on. During the charging of the capacitor, the voltage across it increases exponentially until it reaches to the peak point voltage V_P . Up to now, the UJT is in off state, i.e. non-conducting state at which R_{B1} value is high. When the voltage across the capacitor reaches to peak point voltage (V_P) then, UJT comes into conducting state as the junction is forward biased and R_{B1} falls to low value (50Ω) . Then the capacitor 'C' quickly discharges through UJT that means the discharging time is very less as the capacitor discharges through the low resistance UJT. When the voltage across the capacitor decreases to valley point voltage (V_V) then the UJT shifts to off state and once again the capacitor gets charged through the resistor R and this process is repeated. This generates saw-tooth wave form (Fig.2) across the capacitor which can be viewed on the CRO screen.

We know in RC circuit the instant charge $q = q_0 (1 - e^{-t/RC})$

Multiplying this equation by R\t $\frac{Rq}{t} = \frac{Rq_0}{t} (1 - e^{-t/RC})$

$$RI = RI_0 (1 - e^{-t/RC}) \qquad :: I = q/t$$

$$V = V_0 (1 - e^{-t/RC})$$
 ----- (1) :: RI = V

This is the general equation for voltage in the charging of a capacitor in RC circuit.

But the maximum voltage across the condenser $V_0 = V_{BB}$ and $V = V_P - V_B$

The equation (1) becomes
$$V_P - V_B = V_{BB} (1 - e^{-t/RC})$$

Here, t is the time taken by the condenser to get a charging potential = $(V_P - V_B)$

$$\therefore (1 - e^{-t/RC}) = \frac{V_P - V_B}{V_{RR}} = \eta \quad \text{Where } \eta \text{ is intrinsic stand off ratio.}$$

$$\therefore e^{-t/RC} = (1-\eta)$$

OR
$$\therefore e^{t/RC} = \frac{1}{(1-\eta)}$$

$$t = RC \log_e(\frac{1}{1-\eta}) \quad ---- \quad (2)$$

The time period of the saw tooth wave

T = time of charging + time of discharging

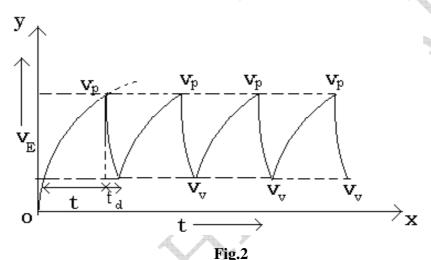
$$T = t + t_d$$

 t_d value is negligibly small. When compared to the value of t, as the discharge takes through the low resistance $R_{\rm B1}$.

$$T \approx t$$
 (3)

From the equations (2) and (3) the time period of the saw tooth wave

$$T = 2.303RC \log_{10}(\frac{1}{1-\eta})$$
 or frequency $f = 1/T$



Procedure:- Connect the circuit as shown in Fig. 1 and apply a fixed voltage V_{BB} (5V to 10V) between the two bases B_1 and B_2 . As the Y – plates of CRO is connected across the condenser a saw tooth wave form is observed on its screen when the power is switch on. Adjust of voltage sensitivity band switch of Y-plates and time base band switch X-plates such that at least one or two waves displayed in the screen. Now note the horizontal length(l) between two successive peaks, in the table. When this horizontal length (l) is multiplied by the time base(t) i.e. \sec/div , we get the time-period(T). The reciprocal of the time-period(1/T) gives the frequency(f). This is the experimental value.

Note the values of resistance R and capacitance C of those connected in the circuit and take the intrinsic stand off ratio η as 0.6, substitute these values in the above formula and find the frequency. This is the theoretical value. Compare the theoretical and experimental frequencies. Repeat the experiment by changing the values of R or C or both.

Precautions:-

- 1) The continuity of the connecting terminals should be checked before going to connect the circuit.
- 2) Identify the two bases and emitter of UJT and connect properly.
- 3) The power supply should be 'on' only when the observations are taken.
- 4) Measure the horizontal length of the wave with out any error.

Table

 $\eta = 0.6$

			Measurement of time period		me	Frequency		
S. No.	R Ω	C F	Horizontal length(l) div.	Time base (t) sec/div	T = lxt Sec.	Experimental f= 1/T	Theoretical $f = \frac{1}{2.303 RC \log_{10}(\frac{1}{1-\eta})} Hz$	
				33				

* * * * *

26. R-C Coupled Amplifier

<u>Aim</u>: To construct a two stage R-C Coupled amplifier, to study the frequency response of the amplifier and to determine the bandwidth.

<u>Apparatus</u>: Two identical n-p-n transistors, power supply (0-15V), signal generator (0-1 MHz), Carbon resistors, Capacitors, a.c.milli-voltmeter and connecting terminals.

Formula: Voltage Gain $(G) = \frac{V_0}{V_i}$

Where $V_0 = Out out voltage$

 V_i = In out voltage

Bandwidth of the amplifier = $f_2 - f_1$ KHz

where f_1 = lower half-power (cut-off) frequency

 f_2 = upper half-power (cut-off) frequency

Description: D.C. power supply, the resistances R_1 , R_2 and R_E provides potential divider biasing and stabilization network. i.e. It establishes a proper operating point to get faithful amplification. R_E reduces the variation of collector current with temperature. The potential divider bias provides forward bias to the emitter junction and reverse bias to the collector junction. Since the emitter is grounded, it is common to both input and output signals. Therefore, the amplifier is common-emitter amplifier. Capacitor C_{in} (= 10 uF) isolates the d.c. component and the internal resistance of the signal generator and couples the a.c. signal voltage to the base of the transistor. The capacitor C_E connected across the emitter resistor R_E is of large value (= 100 uF) offers a low reactance path to the alternating component of emitter current and thus bypasses resistor R_E at audio frequencies.

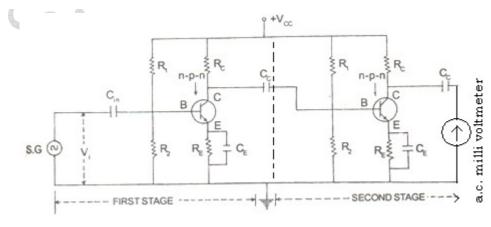


Fig. 1

Consequently, the potential difference across R_E is due to the d.c. component of the current only. The coupling capacitor C_c (= 10 μF) couples the output of the first stage of amplifier to the input of the second stage. It blocks the d.c. voltage of the first stage from reaching the base of the second stage. The output voltage is measured between the collector and emitter terminals.

THEORY:- When a.c. signal is applied to the base of the first transistor, it is amplified and developed across the out of the 1st stage. This amplified voltage is applied to the base of next stage through the coupling capacitor C_c where it is further amplified and reappears across the out put of the second stage. Thus the successive stages amplify the signal and the overall gain is raised to the desired level. Much higher gains can be obtained by connecting a number of amplifier stages in succession (one after the other). Resistance-capacitance (RC) coupling is most widely used to connect the output of first stage to the input (base) of the second stage and so on. It is the most popular type of coupling because it is cheap and provides a constant amplification over a wide range of frequencies. **Fig. 1** shows the circuit arrangement of a two stage RC coupled CE mode transistor amplifier where resistor R is used as a load and the capacitor C is used as a coupling element between the two stages of the amplifier.

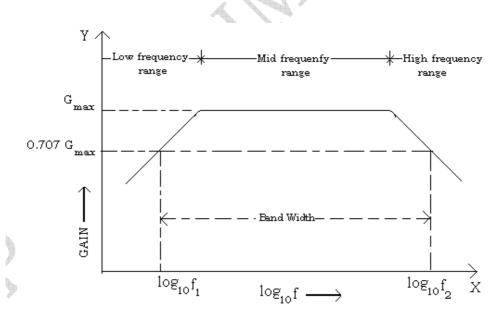


Fig. 2

Frequency response curve

The curve representing the variation of gain of an amplifier with frequency is known as frequency response curve. It is shown in **Fig. 2**. The voltage gain of the amplifier increases

with the frequency, f and attains a maximum value. The maximum value of the gain remains constant over a certain frequency range and afterwards the gain starts decreasing with the increase of the frequency. It may be seen to be divided into three regions. 1) Low frequency range ($<50~\rm{Hz}$) 2) Mid frequency range ($50~\rm{Hz}$ to $20~\rm{KHz}$) and 3) High frequency range ($>20~\rm{kHz}$).

<u>Procedure</u>:- The circuit connections are made as shown in the Fig.1. First the signal generator is connected directly to the a.c. milli-voltmeter by keeping signal frequency at about 500 Hz. The amplitude (voltage) of the in put signal is adjusted to 0.1V or 0.05V. This is the amplifier in put (V_i). Now the signal generator is disconnected from the a.c. milli-voltmeter and connected to the in put of the of the amplifier and the a.c. milli-voltmeter is connected to the out put of the amplifier.

Set the in put frequency at 10 Hz, note the out put voltage (V_o) from the a.c. millivoltmetern keeping the input voltage, V_i constant. Vary the in put frequency 'f' and note the out put voltage. The frequency of the in put signal is varied in convenient steps i.e. at least 5 values with equal intervals, in each range of frequency in the signal generator, the out put voltage V_o is noted in the table for each frequency. Calculate the voltage gain, G of the amplifier for each value of the frequency, f of the input signal, using the relation, Voltage gain, $G = V_o / V_i$.

To determine the bandwidth (BW) of the amplifier

Draw the frequency response curve as said above, by taking the frequency f (or $log_{10}f$) on X-axis and voltage gain on Y-axis. Note the maximum gain, G_{max} and mark the value of $0.707G_{max}$ on the y-axis. From that value draw a line (dashed line) parallel to x-axis. This line cuts the curve at two points, called the half-power points. From those two points draw two perpendicular lines on to x - axis, the feet of two perpendiculars corresponding to two frequencies f_1 and f_2 . These are called as lower half-power frequency and the upper half-power frequency (or cut-off frequency). The difference between these two frequencies f_1 and f_2 is the bandwidth (BW) of the amplifier.

 \therefore Bandwidth of the amplifier = f_2 - f_1

Precautions:-

- 1) Before going to the experiment the in put voltage V_i should be measured.
- 2) The input voltage should be less than 0.1V.
- 3) The in put voltage should be maintained at constant value through out the experiment.
- 4) The connections should be tight.

Table

In put voltage $V_i = V_i$

S.No.	Frequency (f)	Out put Voltage (V _o) V	Log ₁₀ f	$Gain = \frac{V_0}{V_i}$

* * * * *

27.Hartley Oscillator

<u>Aim</u>: To construct Hartley oscillator using a transistor, to find out the frequency of oscillation and comparing it to that of theoretical frequency.

<u>Apparatus</u>:- n-p-n transistor, Carbon resistors (as shown in circuit), two inductors, capacitors, dc power supply, CRO and connecting terminals.

Formulae: The frequency of oscillation of the oscillator $f = \frac{1}{2\pi\sqrt{LC}}$ Hz

Where $L = L_1 + L_2 = Resultant inductance of the series combination.$

 L_1 , L_2 = Self inductances of the two coils (H)

C = Capacitance of the condenser (F)

<u>Description</u>:-The Hartley oscillator is designed for generation of sinusoidal oscillations in the R.F range (20 KHz - 30 MHz). It is very popular and used in radio receivers as a local oscillator.

The circuit diagram of Hartley oscillator (parallel or shunt-fed) using BJT is shown in Figure. It consists of an R-C coupled amplifier using an n-p-n transistor in CE configuration. R_1 and R_2 are two resistors which form a voltage divider bias to the transistor. A resistor R_E is connected in the circuit which stabilizes the circuit against temperature variations. A capacitor C_E is connected in parallel with R_E , acts as a bypass capacitor and provides a low reactive path to the amplified ac signal. The coupling capacitor C_C blocks dc and provides an ac path from the collector to the tank circuit. The L-C feedback network (tank circuit) consists of two inductors L_1 , and L_2 (in series) which are placed across a common capacitor C and the centre of the two inductors is tapped as shown in fig. The feedback network (L_1 , L_2 and C) determines the frequency of oscillation of the oscillator.

THEORY:- When the collector supply voltage V_{cc} is switched on, collector current starts rising and charges the capacitor C. When this capacitor is fully charged, it discharges through coils L_1 and L_2 , setting up damped harmonic oscillations in the tank circuit. The oscillatory current in the tank circuit produces an a.c. voltage across L_1 which *is* applied to the base emitter junction of the transistor and appears in the amplified form in the collector circuit. Feedback of energy from output (collector emitter circuit) to input (base-emitter circuit is) accomplished through auto transformer action. The output of the amplifier is applied across

the inductor L_1 , and the voltage across L_2 forms the feedback voltage. The coil L_1 , is inductively coupled to coil L_2 , and the combination acts as an auto-transformer. This energy supplied to the tank circuit overcomes the losses occurring in it. Consequently the oscillations are sustained in the circuit.

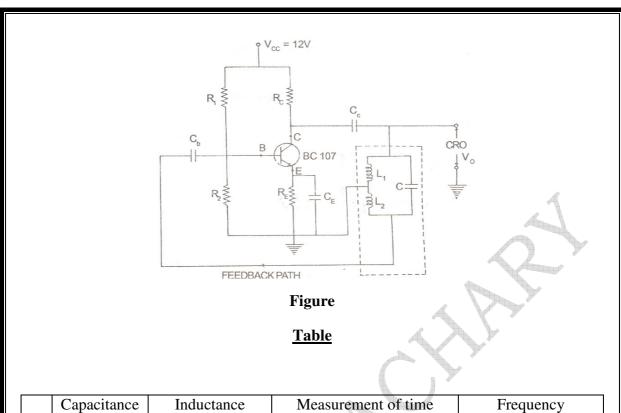
The energy supplied to the tank circuit is in phase with the generated oscillations. The phase difference between the voltages across L_1 and that across L_2 is always 180° because the centre of the two is grounded. A further phase of 180° is introduced between the input and output voltages by the transistor itself. Thus the total phase shift becomes 360° (or zero), thereby making the feedback positive or regenerative which is essential for oscillations. So continuous undamped oscillations are obtained.

<u>Procedure</u>:-The circuit is connected as shown in figure. Connect the CRO across the output terminals of the oscillator. Switch on the power supply to both the oscillator and CRO. Select proper values of C, L_1 and L_2 in the oscillator circuit and get the sine wave form on the screen of CRO. The voltage (deflection) sensitivity band switch (Y-plates) and time base band switch (X-plates) are adjusted such that a steady and complete picture of one or two sine waveform is obtained on the screen. The horizontal length (l) between two successive peaks is noted. When this horizontal length (l), is multiplied by the time base (m) i.e. sec/div, we get the time-period (T = l x m). The reciprocal of the time-period(1/T) gives the frequency (f). This can be verified with the frequency, calculated theoretically by using the above formula. The experiment is repeated by changing C or L_1 or L_2 or all. The readings are noted in the table given.

Precautions:-

- 1) Check the continuity of the connecting terminals before going to connect the circuit.
- 2) Identify the emitter, base and collector of the transistor properly before connecting it in the circuit.
- 3) The horizontal length between two successive peaks should accurately be measured.

Results:	-			



		Capacitance	Inductance		Measurement of time			Frequency	
		(µF)	(mH)		4	period			(Hz)
	S.No.	С	L_1 L_2	$L = L_1 + L_2$	Peak to peak (Horizon tal) length (Div) (l)	Time- base Sec/D iv (m)	Time- perio d T = mxl Sec.	$f = \frac{1}{T}$	$f = \frac{1}{2\pi\sqrt{LC}}$
			3						

* * * * *

28. Colpitt's Oscillator

<u>Aim</u>:- To construct Colpitt's oscillator using a transistor, to find out the frequency of oscillation and comparing it to that of theoretical frequency.

<u>Apparatus</u>: - n-p-n transistor, Carbon resistors (as shown in circuit), inductor, capacitors, dc power supply, CRO and connecting terminals.

Formulae: The frequency of oscillation of the oscillator $f = \frac{1}{2\pi\sqrt{LC}} Hz$

Where L = Self inductance of the coil (H)

C = Capacitance of the condenser (F)

 $C = \frac{C_1 C_2}{C_1 + C_2}$ = Resultant capacitance of the series combination.

 C_1 , C_2 = capacitances of the two capacitors in the tank circuit.

Description: The Colpitt's oscillator is designed for generation of high frequency sinusoidal oscillations (radio frequencies ranging from 10KHz to 100MHz). They are widely used in commercial signal generators up to 100MHz. Colpitt's oscillator is same as Hartley oscillator except for one difference. Instead of using a tapped inductance, Colpitt's oscillator uses a tapped capacitance.

The circuit diagram of Colpitt's oscillator using BJT is shown in Fig. It consists of an R-C coupled amplifier using an n-p-n transistor in CE configuration. R_1 and R_2 are two resistors which form a voltage divider bias to the transistor. A resistor R_E is connected in the circuit which stabilizes the circuit against temperature variations. A capacitor C_E is connected in parallel with R_E , acts as a bypass capacitor and provides a low reactive path to the amplified ac signal. The coupling capacitor C_C blocks dc and provides an ac path from the collector to the tank circuit.

The feedback network (tank circuit) consists of two capacitors C_1 and C_2 (in series) which placed across a common inductor L. The centre of the two capacitors is tapped (grounded). The feedback network (C_1 , C_2 and L) determines the frequency of oscillation of the oscillator. The two series capacitors C_1 , and C_2 form the potential divider led for providing the feedback voltage. The voltage developed across the capacitor C_2 provides regenerative feedback which is essential for sustained oscillations.

THEORY:- When the collector supply voltage V_{cc} is switched on, collector current starts rising and charges the capacitors C_1 and C_2 . When these capacitors are fully charged, they discharge through coil L setting up damped harmonic oscillations in the tank circuit. The oscillatory current in the tank circuit produces an a.c. voltages across C_1 , C_2 . The oscillations across C_2 are applied to base-emitter junction of the transistor and appears in the amplified form in the collector circuit and overcomes the losses occurring in the tank circuit.

The feedback voltage (across the capacitor C_2) is 180° out of phase with the output voltage (across the capacitor C_1), as the centre of the two capacitors is grounded. A phase shift of 180° is produced by the feedback network and a further phase shift of 180° between the output and input voltage is produced by the CE transistor. Hence, the total phase shift is 360° or 0° , which is essential for sustained oscillations, as per, the Barkhausen criterion. So we get continuous undamped oscillations.

<u>Procedure</u>: The circuit is connected as shown in figure. Connect the CRO across the output terminals of the oscillator. Switch on the power supply to both the oscillator and CRO. Select proper values of L, C_1 and C_2 in the oscillator circuit and get the sine wave form on the screen of CRO. The voltage (deflection) sensitivity band switch (Y-plates) and time base band switch (X-plates) are adjusted such that a steady and complete picture of one or two sine waveform is obtained on the screen. The horizontal length (l) between two successive peaks is noted. When this horizontal length (l), is multiplied by the time base (m) i.e. sec/div, we get the time-period (T = 1 x m). The reciprocal of the time-period(1/T) gives the frequency(f). This can be verified with the frequency, calculated theoretically by using the above formula. The experiment is repeated by changing L or C_1 or C_2 or all. The readings are noted in the table given.

Precautions:-

- 1) Check the continuity of the connecting terminals before going to connect the circuit.
- 2) Identify the emitter, base and collector of the transistor properly before connecting it in the circuit.
- 3) The horizontal length between two successive peaks should accurately be measured.

Results	:-
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29. Operational Amplifier as inverting amplifier

<u>Aim</u>: To compare the experimental voltage gain of the operational amplifier with that of the theoretical value and also to observe the in put and the out put are out of phase.

<u>Apparatus</u>: Operational amplifier (IC 741), C.R.O., signal generator, power supply to the amplifier, non inductive resistors of different values and connecting terminals.

Formula:-
$$\frac{e_0}{e_I} = -\frac{R_f}{R_I}$$

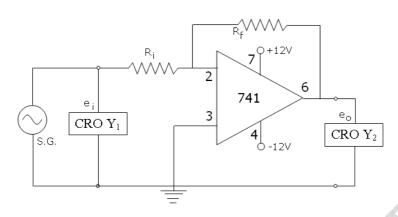
Where e_i and e_o are in put and out put voltages (peak to peak voltages in C.R.O.)

R_i and R_f are in put and feed back resistors.

Description: The heart of an analog computer is the Operational Amplifier. The Operational Amplifier is a stable, high gain DC coupled amplifier which is widely used with a large amount of negative feed back. Many important mathematical operations such as signal addition (or subtraction), differentiation, integration, comparison, isolation, amplification, oscillators, arbitrary function generators etc. are performed in analog computer by using Op-Amp.

An ideal Operational Amplifier would have very high open loop gain, bandwidth and zero noise, off set and drift. The basic circuit block of the amplifier is shown in the Fig. as a triangle with 3 signal terminals. Any signal fed to the inverting input terminal (marked '-') appears amplified at the output with reverse phase, while signal fed to the non-inverting input (marked '+') appears amplified at the output without phase reversal. Now for ideal amplifier in which the input impedance is infinite, no current is drawn from the signal source, and the difference in potential between two input terminals is zero due to infinite gain. But non-ideal amplifier has high voltage gain in the range from 10³ to 10⁷ and input impedance is high and of the order of millions of ohms. So these two conditions are satisfied in the case of non-ideal amplifier also. The amplifier does not distort the waveform of the input voltage regardless of the frequency component. In practice, however, the band width of operational amplifier (namely the range of frequencies of input signal over which A is constant) extends from 0 Hz to few MHz. As the gain of the amplifier equals A at 0 Hz, the amplifier is called direct coupled.

Theory:-Operational Amplifier has odd number of stages for obtaining negative feed back, Since for performing various mathematical operations we need negative feed back.



Inverting amplifier (Fig)

Now from Fig. we can derive closed loop gain (i.e. gain with feed back) for an Operational Amplifier, in the Fig $\,R_f$ is Feed back Resistor. Now applying Kirchoffs current law at place e_g .

We get

$$\frac{e_i - e_g}{R_i} = \frac{e_g - e_0}{R_f} \quad ----- \quad (1)$$

OR

$$\frac{e_i}{R_i} + \frac{e_0}{AR_i} = \frac{-e_0}{AR_f} - \frac{e_0}{R_f} \quad ------ (2)$$

As per the operational amplifier $e_o = -Ae_g$ and putting $e_g = -e_o/A$

OR

$$e_o(\frac{1}{AR_i} + \frac{1}{AR_f} + \frac{1}{R_f}) = -\frac{e_i}{R_i}$$

$$\frac{e_o}{R_f}(\frac{R_f}{AR_i} + \frac{1}{A} + 1) = -\frac{e_i}{R_i}$$

Now R_f/R_i is of the order of 1 to 10 & A= 10^6 .

 $\therefore \frac{R_f}{AR_i}$ and 1/A can be neglected.

There fore the above equation becomes

$$\frac{e_o}{R_f} = -\frac{e_i}{R_i}$$

OR
$$\frac{e_o}{e_i} = -\frac{R_f}{R_i}$$

The ratio = R_f / R_j must not exceed 10. The reason is that greater will be ratio, lesser will be precision. We also see that the output voltage depends only upon the input voltage and values of the two passive

components, namely, the resistors. This implies that the precision by the mathematical operation performance depends only on the precision of the externally connected passive components.

Procedure: The phase terminal of the signal generator is given to the inverting in put (2) of the Op. Amp. IC 741 through an in put resistor R_i . The other terminal of the signal generator and the non-inverting terminal (3) of the amplifier are grounded. The out put (6) of the amplifier is fed back to the in put (2) through a feed back resistor R_f . To measure the I/P and O/P voltages, the signal generator phase terminal and the out put (6) of the amplifier are given to Y_1 and Y_2 plates of the CRO respectively. The other terminals of the CRO are grounded. The terminals 7 and 4 of the op. amp. are connected to +12V and -12V of the power supply.

First the in put resistor R_i (nearly $1K\Omega$), feed back resistor R_f (nearly $2\ K\Omega$ to $10\ K\Omega$) values and in put voltage e_i (0.1V to 0.5V) are fixed. Then observe the input and out put signals on CRO screen. Adjust the time base and vertical gain (volts/div.) of the y_1 and y_2 plates to a convenient value, such that the two signals are stationary and completely observable. Adjust the frequency of the in put signal such that in put and out put signals are out of phase. Measure the in put and out put voltages e_i and e_o (vertical peak to peak) and note the values in the table. The experiment is repeated by changing the values of R_i and R_f .

The theoretical gain $(R_f/R_i$) and experimental gain $(e_o/e_i$) are calculated and compared in the table.

<u>Precautions</u>: 1.Out put of Op. Amp. Can not beyond 15V if so, the Op. Amp. Will go in to saturation state. So do not feed in put more than 1.5 V.

- 2. Adjust the in put frequency such that in put and out put signals are out of phase.
- 3. Check the continuity of the connecting terminals before connecting them.
- 4. See that the ratio = R_f / R_i should not exceed 10

Result	•-			

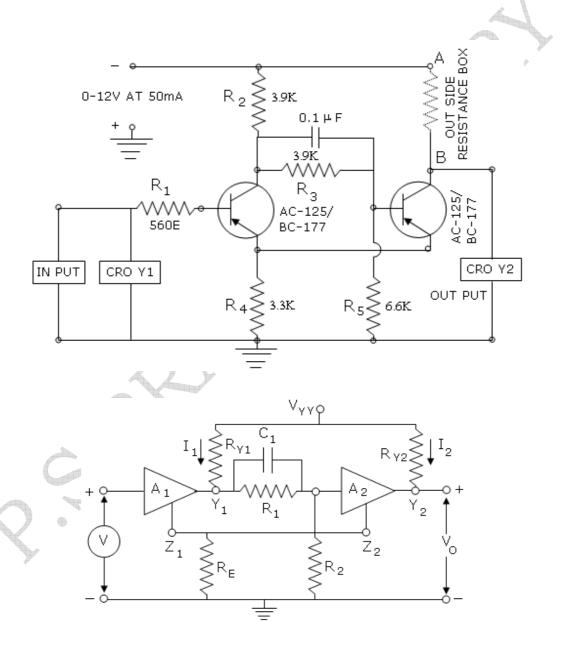
<u>Table</u>				
	in	Experimen tal $(e_{\phi}e_i)$		
	Gain	Theoretic al (R _f /R _i)		
	e _o)	Voltage e _o = nxd (volts)		
	Out put Voltage (e _o)	Voltage Sensitivit y. (Volt/Di		
	Out p	Peak to peak (Vertical) (Divisions)		
	Input voltage (e _i)	Voltage (e;)=nxd (volts)		
		Voltage Sensitivit y. (Volt/Di		
		Peak to peak (Vertical		
*	$R_{ m f}$			
	R _i			
		S. No.		

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30. Schmitt's Trigger

<u>Aim</u>: To get the desired rectangular wave by giving sine wave to the in put of the Schmitt's trigger circuit.

<u>Apparatus</u>:- Signal generator, decade resistance box, cathode ray oscilloscope, a kit containing two transistors (Q_1 and Q_2) of same type, different resistors, capacitor, DC variable power supply as shown in the circuit and connecting terminals.



<u>Theory</u>:- Schmitt trigger circuit is a bi stable multi vibrator and it is named after its inventor.

This Schmitt trigger circuit differs from the basic Eccles – Jordan circuit. The difference is that the coupling from the out put of the second stage to the in put of the first stage is missing

and also the positive feedback is incorporated in to the circuit by coupling through the emitter resistance. The loop gain of the circuit is greater than one. This has two stable states having finite values.

When power is first switched on it gives a small forward bias to Q_2 then it comes in to conducting state. This current flows through R_4 which gives a potential drop V_E across R_4 . This V_E gives reverse bias to the base of Q_1 . So it comes to off state then the voltage across Q_1 will be equal to V_{cc} , and voltage across Q_2 approaches to zero. So in this case.

- a) Q_1 is in cut off state and voltage across it is high.
- b) Q_2 is in saturation or conducting state and voltage across it is low or zero. If the positive voltage of the sine wave from the signal generator is sufficient to over come the reverse bias of Q_1 , then Q_1 comes in to conducting state and the negative going voltage is applied to the base of Q_2 through R_3 . This reduces the forward bias of Q_2 and thus Q_2 comes in to cut-off state. Then the voltage across it is high and voltage across Q_1 is low.

The same process repeats with opposite sense when negative half cycle if in put of a.c. is applied. The combined effect generates a rectangular wave at the out put. Also the frequency of the rectangular wave is equal to the frequency of the a.c. input signal.

The amplitude of the in put voltage required to put Q_2 in to conducting state is called lower trigger potential (LTP). Similarly input voltage required to put Q_1 in to conducting state is called upper trigger potential (UTP).

So, the Schmitt trigger circuit converts any type of wave in to a rectangular wave.

<u>Procedure</u>:- The transistors Q_1 and Q_2 are given connections through different values of resistors as shown in the circuit diagram. The two emitters of Q_1 and Q_2 are inter connected and it is connected to ground through R_4 which gives a feed back. The collectors are given negative voltage and the positive of the supply is grounded. This is a variable power supply. The signal generator is connected to input. Here, the collector Resistance of Q_2 is a variable one. So, a decade resistance box is connected in that Place. The input is connected to Schmitt Trigger circuit. Also, the out put of signal generator is given to Y_1 plates of CRO and the out put of Schmitt Trigger are is given to y_2 plates to observe both in put and out put signals on the screen. First the power supply value V_{cc} & the Resistance value (3KΩ) in the decade Resistance box are fixed. Also the frequency of the signal generator is kept at 1KHz.

Below certain minimum amplitude of input signal no output wave form is observed on the screen of the CRO (y_2) . So, to get the output a minimum amplitude of in put is required. Now increase the amplitude of the input signal above the minimum value, then gate width increases with the increase of amplitude. Note these values in the table-1. But the frequency of the output remains constant. Here, the amplitude of rectangular wave is independent of amplitude of input signal.

In the other case we fix the amplitude of the in put signal above minimum value & the frequency is also fixed. Now, if we increase the resistance in the decade resistance box, the amplitude of the Rectangular wave increases. These values are noted in the table-2. But the frequency doesn't vary with change of resistance.

Precautions:-

- 1) The Time Base of the CRO is selected according to the input signal.
- 2) The V_{cc} value and the Resistance in the box are kept constant through out the experiment for which they are constant.

Result:-

- 1) The frequency of the Rectangular wave is equal to that frequency of input signal.
- 2) The gate width of Rectangular wave can be increased by increasing the amplitude of the input signal.
- 3) The amplitude of the rectangular wave increases with the increase of collector resistance of Q_2 .

Table - 1

Variation of gate width with amplitude of input signal:-

S.No	Applied Voltage (peak voltage) 'v'	Horizontal length 'n'	Time base 't' (sec/div)	Gate width n x t (sec)
				2

Table -2

Variation of amplitude of the square wave with Resistance at constant input amplitude

S.No.	Resistance in the box (Ω)	Vertical height of the square wave (h) div	Voltage sensitivity (volt / div) 'd'	Peak to Peak 2A = h x d 'v'	Amplitude of the square wave $A = 2A/2$

* * * * *

31.Astable Multivibrator (AMV)

<u>Aim</u>: To construct an astable multivibrator using transistors for getting square wave and to determine the frequency of oscillation.

<u>Apparatus</u>: Two n-p-n transistors, two fixed carbon resistors, two variable non – inductive resistors (pots), two capacitors, d.c. power supply, CRO and connecting terminals.

Formula:
$$f = \frac{1}{T} = \frac{1}{0.69(R_1C_1 + R_2C_2)} Hz$$

OR

$$f = \frac{1}{T} = \frac{1}{1.38 \ RC} \ Hz$$
 if $R_1 = R_2 = R$ and $C_1 = C_2 = C$

<u>Description</u>: An astable or free running multivibrator is very important because it generates square waves of its own i.e., without any external excitation. It has no stable state but has only two quasistable (half stable) states between which it keeps on oscillating on its own accord.

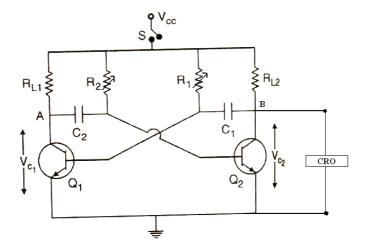


Fig.1

Fig. 1 shows the circuit of a symmetrical collector-coupled astable multivibrator using two identical transistors Q_1 and Q_2 . It, in fact, consists of two common emitter RC coupled amplifier stages. The output of the first stage is coupled to the input of the second stage and the output of the second stage is coupled to the input of the first stage through R and C.

The phase of a signal is reversed when it is amplified by a single stage of a *CE* amplifier. Hence after passing through two stages, it comes back to its original phase. Thus the signal fed back to the base of common emitter transistor is in the same phase as the

original signal at its input. Thus a positive feed back takes place and circuit oscillates. The feedback is so strong that either the transistors are driven to saturation or to cut-off.

THEORY:- When power V_{cc} is applied by closing switch S, collector current starts flowing in Q_1 and Q_2 and the coupling capacitors C_1 and C_2 start charging up. Since the characteristics of no two seemingly similar transistors can be exactly alike, one transistor, say Q_1 will conduct more rapidly than the other. Then the collector current of Q_1 will rise at a faster rate causing a decrease in its collector voltage. The resulting negative signal is applied to the base of Q_2 through C_2 and drives it towards cut-off. Consequently, the collector voltage of Q_2 (positive going signal) is fed to the base of transistor Q_1 through capacitor C_1 . As a result of this positive going pulse, the collector current of Q_1 is further increased. The process being cumulative, in a short time, transistor Q_1 is saturated while Q_2 is cut-off. These actions are so rapid and instantaneous that C_1 does not get a chance to discharge. Under this situation, whole of V_{cc} drops across R_{L1} (since Q_1 is saturated or is in ON state) i.e., $V_{c1} = 0$ and point A is at ground (or zero) potential. Also, since Q_2 is cut-off (OFF state), there is no drop across R_{L2} and point B is at V_{cc} .

Capacitor C_2 now begins to discharge through R_2 , which decreases the reverse bias on base of transistor Q_2 . Ultimately a forward bias is re-established at Q_2 which, therefore, begins to conduct. Consequently, Collector of Q_2 becomes less positive. This negative going voltage signal is applied to the base of transistor Q_1 through the capacitor C_1 . As a result, Q_1 is pulled out of saturation and is soon driven to cut-off. Simultaneously Q_2 is driven to saturation. Now V_{c2} decreases and becomes almost zero volt when Q_2 gets saturated. Consequently, potential of point B decreases from V_{cc} to almost zero volt.

The transistor Q_1 remains cut-off and Q_2 in conduction until capacitor C_1 discharges through R_1 , enough to decrease the reverse bias of Q_1 The whole of the cycle is repeated.

The output of the multivibrator can be taken from the collector of either transistor. The output is a square wave, as shown in Fig. 2 with a peak amplitude equal to V_{cc} .

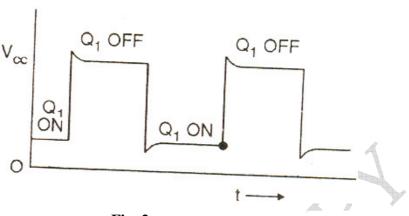


Fig. 2

Switching Times

It is seen that the multivibrator circuit alternates between a state in which Q_1 is ON and Q_2 is OFF and a state in which Q_1 is OFF and Q_2 is ON. The time for which either transistor remains ON or OFF is given by :

ON time for Q_2 (or OFF time for Q_1) $T_1 = 0.69 R_1 C_1$

ON time for Q_1 (or OFF time for Q_2) $T_2 = 0.69 R_2 C_2$

Hence, total time of the square wave $T = T_{1+}T_2$

$$= 0.69 (R_1C_1 + R_2C_2)$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$ i.e., the two stages are symmetrical, then

$$T = 0.69 (RC + RC) = 1.38 RC$$

Frequency of Oscillation: Frequency of the square wave is given by the reciprocal of the

time period i.e $f = \frac{1}{T} = \frac{1}{1.38 \ RC} \ Hz$

Procedure: The two transistors (Q_1 and Q_2) are connected in CE mode and they are given proper bias with the help of R_{L1} , R_{L2} and + V_{CC} . Collector of each transistor is connected to the base of the other transistor through a condenser. The condensers C_1 and C_2 are connected to the power supply through the variable resistors R_1 and R_2 . The collector of any one of the transistor is connected the Y – plates of CRO.

Switch on the power V_{cc} , and the power supply of CRO. Observe the square wave on the screen. Adjust the values R_1 and R_2 and the band switches of X and Y plates of CRO to get at least one complete wave on the screen.

Then the length of one complete wave (1) on screen is measured on horizontal scale, this is multiplied with the time base (t). The product will give the time period of the wave ($1 \times t = T$). The reciprocal of 'T' gives the frequency (f). These values are noted in the table. This frequency is experimental frequency.

Now the Power V_{cc} is switched off and the resistance values of R_1 and R_2 are measured using multi-meter. The values R_1 , R_2 , C_1 and C_2 are also noted in the table. Substituting these values in the above formula we will get the frequency theoretically. The theoretical and experimental frequencies are compared. They are equal.

The experiment is repeated with different values of R_1 and R_2 (the values of C_1 and C_2 can also be changed, if possible).

Precautions:-

- 1) Select the two transistors such that they are identical.
- 2) Before going to the experiment the emitter, collector and base terminals of the two transistors should be identified properly.
- 3) The gain band switch of Y plates and band switch of time base are kept in proper position to observe at least one complete wave on the screen of CRO.

$$\begin{array}{cccc} & & & & & \\ \hline \textbf{Table} & & & & \\ C_1 & = & & \mu F & & & \\ C_2 & = & & \mu F & & \\ \end{array}$$

	Resis es	stanc	Time perio CRO	d measuremen	nt using	Freq	uency (Hz)
S. No	R_1 Ω	$egin{array}{c} R_2 \ \Omega \end{array}$	Horizont al length (1) div.	Time base (t) Sec/ div.	T = 1 x t Sec.	Experiment al f = 1/T	Theoritical $f = 1/0.69(R_1C_1+R_2C_2)$
) •						

* * * * *

32. Operational Amplifier as astable multivibrator

<u>Aim</u>:- To construct an astable multivibrator using operational amplifier 741 for getting square wave and to determine the frequency of oscillation and comparing it with that of theoretical value.

<u>Apparatus</u>:- Operational amplifier (IC 741), C.R.O., two power supplies to the operational amplifier, two non inductive fixed resistors (R_1 and R_2), one non-inductive variable resistor(R_2), capacitor and connecting terminals.

Formula:- Time period of the square wave

$$T = 2 \times 2.303 \text{ RC } \log_{10} \left(\frac{2R_1 + R_2}{R_2}\right) \text{ Sec}$$

Where $R, R_1 \text{ and } R_2 = \text{Resistances } (\Omega)$

 $C = Capacitance (\mu F)$

 \therefore Frequency of the square wave $f = \frac{1}{T} Hz$

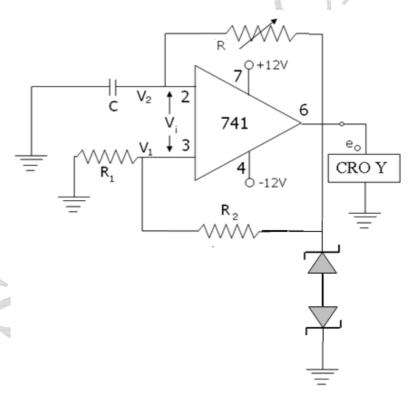


Fig - 1

Description: An astable multi vibrator or free running multi vibrator generates square waves of its own i.e. without any external excitation. It has no stable state but has only two quasi stable (half stable) states between which it keeps on oscillating on its own accord.

<u>Fig-1</u> is the circuit of the astable multi vibrator. A capacitor C is connected to the inverting terminal (2) of the operational amplifier from the ground. Similarly a resistance R_1 is connected to the non-inverting terminal (3) of the operational amplifier from the ground. The output terminal (6) of the amplifier is fed back to inverting and non-inverting terminals of operational amplifier through resistors R and R_2 respectively. Here R_2 is fixed resistor and R is variable resistor. To observe the out put wave form, the out put terminal (6) is connected to CRO Y- Plates phase terminal and the other terminal of CRO is grounded. The terminals (7) and (4) of the op. amp. are connected to +12 V and -12 V of the D.C. power supplies separately. The out put terminal (6) is also grounded through a series combination of two zener diodes connected in reverse order as shown in the fig-1.

Theory:- First the inverting terminal (2) is at zero potential ($V_2 = 0$, the inverting terminal 2 is virtually grounded) and the input at the non-inverting terminal (3) has some potential V_1 i.e the voltage across R_1 . This occurs due to the power supply of the operational amplifier. The potential difference between the two input terminals (inverting and non-inverting terminals) is

$$\begin{aligned} V_i &= V_1 - V_2 \\ &= V_1 - 0 \\ &= V_1 \qquad \text{Here } V_1 \text{ is +ve. } (\because V_2 = 0) \end{aligned}$$

This '+ ve' voltage drives the output of operational amplifier into '+ ve' saturation voltage ($+V_{sat}$). This large saturation voltage is due to the high gain of the operational amplifier i.e. the comparator character of the amplifier. When the + V_{sat} is fed back to the inverting terminal (2) through the resistor R, the capacitor C gets charged and the potential of the right side plate of the capacitor gradually rises (or) the V_2 value rises (Even though the inverting terminal 2 is virtually grounded but it is not mechanically grounded). When V_2 becomes slightly more than V_1 , the in put ($V_1 = V_1 - V_2$) becomes '-ve' and immediately this '-ve' voltage drives the out put of the operational amplifier in to '-ve' saturation voltage ($-V_{sat}$).

Now the capacitor discharges gradually. When V_2 becomes less than V_1 and $(V_1 - V_2)$ becomes '+ve' and the out put drives to + V_{sat} . The same process is repeated and the out put of the operational amplifier swings between two saturation voltages i.e. between + V_{sat} and - V_{sat} . The out put e_o of the operational amplifier is square wave. So, operational amplifier can function as a square wave generator. The wave shape is as shown in Fig-2.

The duration of saturation is

$$t = \frac{T}{2} = \text{RC log}_{e} \left(\frac{1+\beta}{1-\beta}\right) \text{ Sec}$$

Where

 $\beta = (\frac{R_1}{R_1 + R_2})$ = Feed back factor

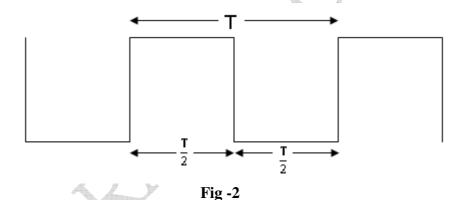
Then

$$t = \frac{T}{2} = RC \log_e (\frac{2R_1 + R_2}{R_2}) Sec$$
(OR)

$$T = 2 \times 2.303 \text{ RC } \log_{10} \left(\frac{2R_1 + R_2}{R_2} \right) \text{ Sec}$$

(Note : If $R_1 = R_2$ then T = 2.1976 RC

From this the frequency of oscillation $f = \frac{1}{T}$ Hz can be calculated.



<u>Procedure</u>: Connect the circuit as shown in the Fig-1. Take the $R_1 = R_2 = 1K\Omega$, $C = 0.1\mu Fand R = 10K\Omega$ (variable resistance) or any convenient values. Apply the DC power supplies to the terminals (7) and (4) of the operational amplifier. Keep the R_2 value at a convenient value. Set the voltage sensitivity band switch of the Y- plate and time base band switch of C.R.O. to the convenient positions such that at least two or more complete square wave forms are observed on the screen of CRO. Now measure the horizontal length (l) of one complete wave form as shown in the <u>Fig-2</u>. Also note the time base value (m) in the table. From this calculate the time period and frequency of the square wave as per the table. This is the experimental frequency. Similarly the theoretical frequency can also be calculated by substituting the values of R, R_1 , R_2 and C in the above given equation.

Now the experiment is repeated for different values of R by increasing its value in equal steps (Multiples of $100\,\Omega$).

Precautions:-

- 1) Check the continuity of the connecting terminals before connecting them.
- 2) Keep the band switches of the C.R.O. such that steady wave forms are observed on the screen.
- 3) Observe the out put square wave on the screen of CRO and measure the horizontal length accurately.

Results:- It is found that the observed frequency and calculated frequency are equal.

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33. Operational Amplifier as differentiator

<u>Aim</u>: To study the gain of the OP. amp. as differentiator with the frequency of the in put, to compare the experimental out put with that of theoretical value. Also to observe the differentiating character of the circuit.

<u>Apparatus</u>:- Operational amplifier (IC 741), C.R.O., signal generator, power supply to the amplifier, non inductive resistor, capacitor and connecting terminals.

Formula: Out put voltage $V_o = -R C \omega V_{ip} Cos \omega t$ (OR) Out put peak voltage $V_{op} = -R C \omega V_{ip}$

Where $R = Resistance(\Omega)$

C = Capacitance(F)

 ω = Angular frequency of the in put (Rad/sec) = $2\pi f$

f = Frequency of the in put (Hz)

Description: The phase terminal of the signal generator is given to the inverting in put (2) of the operational amplifier 741 through a capacitor C. The other terminal of the signal generator and the non-inverting terminal (3) of the op. amp. are grounded. The out put terminal (6) of the op.amp. is fed back to the inverting terminal (2) through a resistor R. To measure the in put and out put voltages, the signal generator phase terminal and the out put terminal (6) of the op. amp. are connected to the phase terminals of Y_1 and Y_2 plates of C.R.O. respectively. The other two terminals of the C.R.O. are grounded. The terminals 7 and 4 of the op. amp. are connected to +12 V and -12 V of the D.C. power supplies separately.

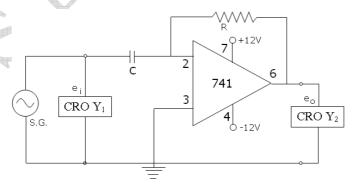
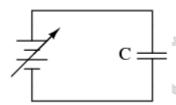


Fig – 1

Theory:- A circuit that performs the mathematical differentiation of the in put signal is called a "differentiator". i.e. the out put of the differentiator is proportional to the rate of change of its in put signal. By introducing electrical reactance (resistance or capacitance) into the feedback loops of op-amp amplifier circuits, we can cause the output to respond to changes in the input voltage with time.

Capacitance can be defined as the measure of a capacitor's opposition to changes in voltage. The greater the capacitance, the more the opposition. Capacitors oppose voltage change by creating current in the circuit, i.e. they either charge or discharge in response to a change in applied voltage. So, the more capacitance a capacitor has, the greater its charge or discharge current will be for any given rate of change of voltage across it.



The equation for this is $I = C \frac{dV_i}{dt}$

We can build an op-amp circuit which measures change in voltage by measuring current through a capacitor, and outputs a voltage proportional to that current.

The right-hand side of the capacitor is held to a voltage of 0 volts, due to the "virtual ground" effect(This terminal is not mechanically grounded. So no current flows to ground through this terminal). Therefore, current "through" the capacitor is only due to *change* in the input voltage. A steady input voltage won't cause any current through C.

Capacitor current moves through the feedback resistor, producing a drop across it, which is the same as the output voltage. A linear, positive rate of input voltage change will result in a steady negative voltage at the output of the op-amp.

∴ The out put voltage

$$V_o = -IR$$

$$V_o = -RC \frac{dV_i}{dt}$$

If in put voltage $V_i = V_{ip} \sin \omega t$ Here $V_{ip} = \text{In put peak voltage}$

Then
$$V_o = -RC \frac{d(V_{ip} Sin \omega t)}{dt}$$

$$V_o = -V_{ip}RC\omega Cos(\omega t)$$

OR

The peak out put voltage $V_{op} = -R C \omega V_{ip} = -R C 2\pi f V_{ip}$

Conversely, a negative rate of input voltage change will result in a steady positive voltage at the output of the op-amp. This polarity inversion from input to output is due to the fact that the input signal is being sent (essentially) to the inverting input of the op-amp, so it acts like the inverting amplifier.

- The out put voltage increases with increasing frequency or the differentiator circuit has high gain at high frequencies.
- ➤ When there is change in the in put then only the out put occurs.
- ➤ If the in put is constant the out put is zero.

Procedure:- Connect the circuit as shown in the fig-1. Take the $R=1K\Omega$ and $C=0.1\mu F$ or any convenient values. Apply the sine wave from the signal generator to the op. amp. Set the frequency of the signal generator i.e. in put frequency to 1 KHz. Also set the in put peak to peak in put voltage to a fixed value by adjusting the voltage sensitivity band switch of the Y_1 -plates and time base band switch of C.R.O. to the convenient positions. The voltage of Y_1 -plates on the C.R.O. screen is noted in the table as V_{ip} . Now observe the out put voltage at the Y_2 - plates of C.R.O. Also keep the voltage sensitivity band switch of Y_2 plates at convenient position.

Now the input frequency is increased in equal steps (Multiples of 100 Hz) and the out put voltage is measured for each frequency. Note in put frequency(f), in put voltage (V_{ip}) and out put voltage (V_{op}) in the table. The out put peak voltage (V_{op}) is compared with that of theoretical value. The gain increases with increase of in put frequency. This one character of the differentiator.

The other character is that the out put occurs only when there is change in the in put voltage. To observe this, square wave is applied as in put. Then the out put pulses are observed only at the phase reversal time and no voltage is observed in between.

Precautions:-

- 1) Check the continuity of the connecting terminals before connecting them.
- 2) Keep the band switches of the C.R.O. such that steady wave forms are observed on the screen.
- 3) Observe the in put and out put voltages simultaneously on the screen when square wave is applied in order to know that the out put occurs only when there is change in the in put.

Results :-

- 1. The out put voltage increases with increasing frequency or the differentiator circuit has high gain at high frequencies.
- 2. When there is change in the in put then only the out put occurs.
- 3. If the in put is constant the out put is zero.

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34. Operational Amplifier as mono stable multi vibrator

<u>Aim</u>: To construct a monostable multivibrator using operational amplifier 741 and to determine the duration of the output pulse generated and to compare it with that of theoretical value.

<u>Apparatus</u>:- Operational amplifier (IC 741), C.R.O., two power supplies to the operational amplifier, four non inductive fixed resistors (R_1 , R_2 , R_4 and R_5), one non-inductive variable resistor(R_3), two capacitors(C_1 and C_2), three diodes (D_1 , D_2 and D_3) and connecting terminals.

Formula: Duration of the output pulse generated or time duration of quasi-stable state

$$T = 2.303 \text{ x } R_3C_1 \log_{10} \left(\frac{R_1 + R_2}{R_1}\right) \text{ Sec}$$

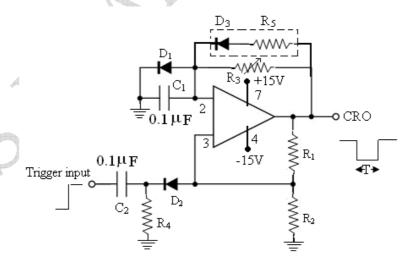
Where R_1 and R_2 = Fixed non-inductive resistances (Ω)

 R_3 = Variable non-inductive resistance (Ω)

 C_1 = Capacitance (μ F)

and if $R_1 = R_2$

Then $T = 0.693 R_3 C_1$



Figure

Description: The above figure is the circuit of the monostable multi vibrator. A capacitor C_1 is connected to the inverting terminal (2) of the operational amplifier from the ground and a diode D_1 is connected in parallel to C_1 such that n of diode D_1 is grounded. Similarly a series combination of a capacitor C_2 another diode D_2 is connected to the non-inverting

terminal (3) of the operational amplifier as shown in the figure. The junction of C_2 and D_2 is grounded through a resistor R_4 . The in put external triggering pulse is given to the capacitor C_2 . The output terminal (6) of the amplifier is fed back to inverting and non-inverting terminals of operational amplifier through resistors R_3 and R_1 respectively. Here R_1 is fixed resistor and R_3 is variable resistor. For the <u>fast recovery</u> of the multivibrator, from the quasistable state, a series combination of a diode D_3 and a resistor R_5 is connected parallel to the resistor R_3 . The non- inverting terminal (3) is also grounded through another resistor R_1 so as the combination of R_2 and R_1 acts as a potential divider for the feed back. The terminals (7) and (4) of the op. amp. are connected to +15 V and -15 V of the D.C. power supplies separately. To observe the out put wave form, the out put terminal (6) is connected to CRO Y- Plates phase terminal and the other terminal of CRO is grounded. Also observe that $(R_5 \le R_3)$ and $(R_4 > R_1)$.

<u>Theory</u>: Multivibrators are a group of regenerative circuits that are used extensively in timing applications. They are wave shaping circuits which give symmetric or asymmetric square out put. They have two states either stable or quasi-stable depending on the type of the multivibrator.

There are three types of multivibrator. 1) **Astable** (free-running) **2) Monostable** (one shot) and 3) **Bistable** (flip-flop).

All the three circuits operate by using positive feedback to drive the op-amp into saturation, therefore it is not the case that the two inputs of the op-amp can be assumed to be at the same potential.

<u>Astable Multivibrator</u>: It is a free running oscillator having <u>two quasi-stable states</u>. Thus there is oscillations between these two states and <u>no external signals are required</u> to produce the change in state. In this the two states are stable only for a limited time and the circuit switches between them with the output alternating between positive and negative saturation values.

Monostable Multivibrator: A monostable multivibrator (MMV) has one stable state and one quasi-stable state. The circuit remains in its stable state till an external triggering pulse causes a transition to the quasi-stable state. The circuit comes back to its stable state after a time period T. Thus it generates a single output pulse in response to an input pulse and is referred to as a one-shot or single shot. An external trigger signal generated due to charging and

discharging of the capacitor produces the transition to the original stable state. So, mono stable multi vibrator is one which generates a single pulse of specified duration in response to each external trigger signal.

<u>Bistable Multivibrator</u>: It maintains a given out put voltage level unless an external trigger signal is applied. Application of an external trigger signal causes a change of state, and this out put level is maintained indefinitely until a second trigger is applied. Thus <u>it requires two external triggers</u> before it returns to its initial state. So, it has <u>two stable states</u>.

Monostable multivibrator circuit illustrated in figure is obtained by modifying the <u>astable multivibrator</u> circuit by connecting a diode D_1 across capacitor C_1 so as to clamp V_c at V_d during positive excursion. The main component of this circuit is the 741, a general-purpose operational amplifier. This is a timing circuit that changes state once triggered, but returns to its original state after a certain time delay. It got its name from the fact that only one of its output states is stable.

Under steady-state condition, this circuit will remain in its stable state with the output V_{out} = + V_{out} and the capacitor C_1 , is clamped at the voltage V_D (on-voltage of diode, D_1 , i.e. V_D = 0.7 V). The voltage V_D must be less than (β V_{out}) for V_{in} < 0. The circuit can be switched to the other state by applying a negative pulse with amplitude greater than (β V_{out} – V_D) to the non-inverting (+) input terminal.

When a trigger pulse with amplitude greater than $(\beta\ V_{out} - V_D)$ is applied, V_{in} goes positive causing a transition in the state of the circuit to $-V_{out}$. The capacitor C_1 now charges exponentially with a time constant $\tau = R_3C_1$ toward $-V_{out}$ (diode D_l being reverse-biased). When capacitor voltage V_c becomes more negative than $(-\beta\ V_{out})$, V_{in} becomes negative and, therefore, output swings back to $+V_{out}$ (steady- state output). The capacitor now charges towards $+V_{out}$ till V_c attain V_D and capacitor C_1 becomes clamped at V_D .

The width of the trigger pulse T_p is much smaller than the duration of the output pulse T_p generated i.e. $T_P \ll T$. For reliable operation the circuit should not be triggered again before T.

During the <u>quasi-stable</u> state, the capacitor voltage is given as

$$V_c = -V_{out} + (V_{out} + V_D) e^{-t/\tau}$$

At instant

t = T and $V_c = -\beta V_{out}$

$$\beta = \left(\frac{R_2}{R_1 + R_2}\right) = \text{Feed back factor}$$
So
$$-\beta \, V_{out} = -V_{out} + (V_{out} + V_D) \, e^{-T/\tau}$$
Where
$$\text{Time constant } \tau = R_3 C_1$$
or
$$V_{out} \, (1 - \beta) = V_{out} \, (1 + \frac{V_D}{V_{out}}) \, e^{-T/\tau}$$
In general
$$V_D << V_{out}$$
So
$$(1 - \beta) = e^{-T/\tau}$$

$$\frac{T}{\tau} = \log_e \, \frac{1}{(1 - \beta)}$$

$$T = R_3 C_1 \log_e \left(\frac{R_1 + R_2}{R_1} \right)$$

 $T = R_3C_1 \log_e \frac{1}{(1-\beta)} \quad \because \tau = R_3C_1$

and if
$$R_1 = R_2$$

Then
$$\beta = \frac{1}{2}$$

Or
$$T = R_3C_1 \log_e 2 = R_3C_1 \times 2.303 \times \log_{10} 2$$

 $T = 0.693 R_3 C_1$

shown in the figure. Take the $R_1 - R_2 - 1KO$, $C_1 - C_2 - 1KO$

<u>Procedure</u>:- Connect the circuit as shown in the figure. Take the $R_1 = R_2 = 1K\Omega$, $C_1 = C_2 = 0.1\mu F$ and $R_3 = 10K\Omega$ (variable resistance) or any convenient values. Apply the DC power supplies to the terminals (7) and (4) of the operational amplifier. Keep the R_3 value at a convenient value. Set the voltage sensitivity band switch of the Y- plate and time base band switch of C.R.O. to the convenient positions such that at least two or more complete square wave forms are observed on the screen of CRO. The length of –ve value or –V_{out} is the duration of the quasi-stable state. Now measure the horizontal length (1) of the quasi-stable state. Also note the time base value (m) of the X-plates of the CRO in the table. From this calculate the time duration of the quasi- stable state. This is the experimental value. Similarly the theoretical value can also be calculated by substituting the values of R_3 , R_1 , R_2 and C_1 in the above given equation.

Now the experiment is repeated for different values of R_3 by increasing its value $\,$ in equal steps (Multiples of 100 Ω).

Precautions:-

- 1) Check the continuity of the connecting terminals before connecting them.
- 2) Keep the band switches of the C.R.O. such that steady wave form is observed on the screen.
- 3) Observe the out put square wave on the screen of CRO and measure the horizontal length accurately.

Results:- It is found that the observed duration and calculated duration are equal.

$$\begin{array}{ccc} & \underline{Table} \\ \\ R_1 = & \Omega & R_2 = & \Omega \end{array}$$

			Theoritical time duration	Experi	mental time	duration
S.No.	\mathbf{C}_1	R_3	$T = P_1C_1 \log \left(\frac{R_1 + R_2}{R_1 + R_2}\right)$	Horizontal	Time base	Time
3.110.	(µF)	(Ω)	$I - R_3C_1 \log_e \left(\frac{R_1}{R_1}\right)$	length (l)	(m)	$T = (1 \ x \ m)$
			$T = R_3C_1 \log_e \left(\frac{R_1 + R_2}{R_1}\right)$ (Sec)	(Div)	Sec/div	(Sec)

* * * * *

35. Wien bridge Oscillator

<u>Aim</u>:- To construct Wien bridge oscillator using operational amplifier 741. To measure the frequency of oscillation and to compare it to that of theoretical value.

<u>Apparatus</u>: Operational amplifier 741, CRO, two variable capacitors (C_1, C_2) , three variable non-inductive resistors $(R_1, R_2 \text{ and } R_3)$ and one fixed resistor, two power supplies and connecting terminals.

Formula:- Frequency of oscillation

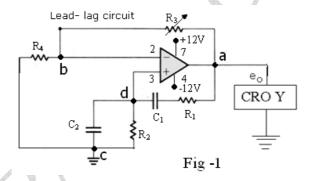
$$f = \frac{1}{2\pi RC} Hz$$

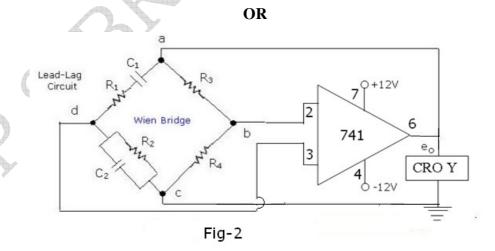
Where

 $R_1 = R_2 = R = Resistances (\Omega)$

and

 $C_1 = C_2 = C = Capacitances (\mu F)$





<u>Description</u>:- Fig-1 or Fig-2 is the circuit of the Wien bridge oscillator (as these two circuits are same). A resistor R_4 is connected to the inverting terminal (2) of the operational amplifier

from the ground. Similarly a parallel combination of a resistance R_2 and a capacitor C_2 is connected to the non-inverting terminal (3) of the operational amplifier from the ground. The output terminal (6) of the amplifier is fed back to inverting terminal (2) through a variable resistor R_3 . A series combination of a resistance R_1 and a capacitor C_1 is connected between non-inverting terminal (3) and the out put of operational amplifier. To observe the out put wave form, the out put terminal (6) is connected to CRO Y- Plates phase terminal and the other terminal of CRO is grounded. The terminals (7) and (4) of the op. amp. are connected to +12 V and -12 V of the D.C. power supplies separately.

Theory:-An oscillator consists of an amplifier and a feedback network.

- 1) 'Active device' i.e. Op Amp is used as an amplifier.
- 2) Passive components such as R-C or L-C combinations are used as feed back net work.

To start the oscillation with the constant amplitude, positive feedback is not the only sufficient condition. Oscillator circuit must satisfy the following two conditions known as **Barkhausen** conditions:

- i. The first condition is that the magnitude of the loop gain $(A\beta) = 1$ A = Amplifier gain and $\beta = Feedback$ gain.
- ii. The second condition is that the phase shift around the loop must be 360° or 0° .

The feedback signal does not produce any phase shift. This is the "basic principle of a Wien bridge oscillator".

<u>Lead-Lag circuit</u>:- The given circuit shows the RC combination used in Wien bridge oscillator. This circuit is also known as lead-lag circuit. Here, resistor R_1 and capacitor C_1 are connected in the series while resistor R_2 and capacitor C_2 are connected in parallel.

Working of lead-lag circuit :- At high frequencies, the reactance of capacitor C_1 and C_2 approaches zero. This causes C_1 and C_2 appears short. Here, capacitor C_2 shorts the resistor R_2 . Hence, the output voltage Vo will be zero since output is taken across R_2 and C_2 combination. So, at high frequencies, circuit acts as a 'lag circuit'.

At low frequencies, both capacitors act as open because capacitor offers very high reactance. Again output voltage will be zero because the input signal is dropped across the R_1 and C_1 combination. Here, the circuit acts like a 'lead circuit'.

But at one particular frequency between the two extremes, the output voltage reaches to the maximum value. At this frequency only, resistance value becomes equal to capacitive

<u>reactance and gives maximum output.</u> Hence, this particular frequency is known as <u>resonant</u> frequency or oscillating frequency.

The maximum output would be produced if $\mathbf{R} = \mathbf{X}\mathbf{c}$

$$R = X_c = \frac{1}{2\pi f C}$$

If $R_1 = R_2 = R$ and $C_1 = C_2 = C$

Then the resonant frequency

$$f = \frac{1}{2\pi RC} Hz$$

Due to limitations of the op-amp, frequencies above 1MHz are not achievable.

The basic version of Wien bridge has four arms. The two arms are purely resistive and other two arms are frequency sensitive arms. These two arms are nothing but the lead-lag circuit. The series combination of R_1 and C_1 is connected between terminal a and d. The parallel combination of R_2 and C_2 is connected between terminal d and c. So the two circuits (Fig.1 and Fig.2) are same except in shape.

Here, bridge does not provide phase shift at oscillating frequency as one arm consists of lead circuit and other arm consists of lag circuit. There is no need to introduce phase shift by the operational amplifier. Therefore, non inverting amplifier is used.

Procedure:- Connect the circuit is as shown in the Fig-1. Keep the resistance and capacitor values $R_1 = R_2 = R$ and $C_1 = C_2 = C$ and switch on the power. Adjust the voltage sensitivity band switch and time – base band switch such that at least two or more complete sine waves are observed on the screen of CRO. Also adjust the resistance R_3 value till the wave formed on the CRO screen is stationary. Note R and C values in the table and measure the peak to peak horizontal length (l) of one sine wave. Multiply this value with the corresponding time-base (t) value. This product (1 x t) gives the time period (T) of the generated sine wave. The reciprocal of time period gives the experimental frequency of the sine wave. On substitution of Rand C values in the above equation, it gives theoretical frequency. The theoretical and experimental frequencies are equal. The experiment is repeated by changing the value of R or C.

Precautions:-

- 1. Check the continuity of the connecting terminals before connecting them.
- 2. Keep the band switches of the C.R.O. and adjust the value of R_3 such that steady wave forms are observed on the screen.
- 3. Observe the out put sine wave on the screen of CRO and measure the horizontal length accurately.

<u>Results</u>:- It is found that the experimental frequency and theoretical frequency are equal.

Table

				6			
	The	oretical frequen	су	Measur	rement of ou	t put frequen	ісу
S.No.	$R_1 = R_2 = R$ (Ω)	$C_1 = C_2 = C$ (μF)	$f = \frac{1}{2\pi RC}$ (Hz)	Peak to peak Horizontal length (l) (Divisions)	Time base (t) Sec/div	Period T=(1 x t) Sec	Frequency $f = \frac{1}{T} Hz$
		35					

36. Amplitude modulation and demodulation

Aim: 1) To superimpose the audio signal on to the carrier wave to get modulated wave.

- 2) To calculate the modulation index from the in put wave and out put wave and comparing them.
- 3) To extract (demodulate) the audio signal from the modulated wave to compare the frequencies and amplitudes of in put audio signal and demodulated wave.

<u>Apparatus</u>:- Two signal generators, two CROs, two NPN transistors, transformer, two capacitors, five resistors, power supply and connecting terminals.

Formulae: 1. Modulation index $M_1 = \frac{b}{a}$

Where b = Amplitude of the signal or audio wave

a = Amplitude of the carrier wave

2. Modulation index $M_2 = \frac{E_{cmax} - E_{cmin}}{E_{cmax} + E_{cmin}}$

Where E_{cmax} =Maximum peak to peak amplitude of the modulated wave

 E_{cmin} = Minimum peak to peak amplitude of the modulated wave

<u>Description</u>:- In the circuit(Fig-1) of amplitude modulation two NPN transistors (T1 and T2) are connected in series such that the collector of T2 is connected to the emitter of T1. The two transistors are provided voltage divider bias with help of resistors and $+V_{cc}$. The carrier wave is fed to the base of the transistor T1 through a capacitor. The capacitor can filter dc, if any, in the ac carrier wave. So pure ac carrier wave reaches to the base of T1. Similarly an audio wave from a signal generator is given to the base of T2 through a resistor in series with a capacitor. Here to measure the in put signal CRO Y1- plates are connected in parallel to the audio signal generator. The emitter current of T1 is the collector current of T2. This collector current Of T2 is as per the audio signal strength. The collector current of T1 is the sum of the currents of emitter and base of T1. So the collector current is the combination of carrier wave and audio signal which is nothing but modulated signal. This modulated wave is given to the Y2 – plates of the CRO through an audio transformer which is connected in parallel to a capacitor.

The other part of the experiment is demodulation. To demodulate the modulated wave the circuit is connected as shown in the Fig-2. In this circuit a parallel combination of a

 $^{\mathrm{age}}134$

<u>Theory</u>:- Amplitude modulation (AM) is a technique used in electronic communication, most commonly for transmitting information via a <u>radio carrier wave</u>. AM works by varying the strength of the transmitted signal in relation to the information being sent.

As originally developed for the electric telephone, amplitude modulation was used to add audio information to the low-powered direct current flowing from a telephone transmitter to a receiver. As a simplified explanation, at the transmitting end, a telephone microphone was used to vary the strength of the transmitted current, according to the frequency and loudness of the sounds received. Then, at the receiving end of the telephone line, the transmitted electrical current affected an electromagnet, which strengthened and weakened in response to the strength of the current. In turn, the electromagnet produced vibrations in the receiver <u>diaphragm</u>, thus closely reproducing the frequency and loudness of the sounds originally heard at the transmitter.

In contrast to the telephone, in radio communication what is modulated is a continuous wave radio signal (carrier wave) produced by a radio transmitter. In its basic form, amplitude modulation produces a signal with power concentrated at the carrier frequency and in two adjacent side bands. This process is known as heterodyning. Each sideband is equal in bandwidth to that of the modulating signal and is a mirror image of the other. Amplitude modulation that results in two side bands and a carrier is often called *double sideband amplitude modulation* (DSB-AM). This is the process taking place at the transmitting end.

At the receiving end the modulated signal is taken as the in put in to the receiver and the receiver extracts the original wave from the modulated wave and gives it as out put. This is the process of demodulation.

Modulation index

It is the measure of extent of amplitude variation about an demodulated maximum carrier. This quantity is also called as *modulation depth* and it indicates by how much the modulated variable varies around its 'original' level. For AM, it relates to the variations in the carrier amplitude. We compare the modulation indices both at the in put level and out put level as shown in the above equations.

Fig - 3

Procedure: The circuit is connected as shown in the Fig-1 for producing amplitude modulated wave. The frequency of the carrier wave is in MHz. First measure the peak to peak (2a) vertical voltage of the carrier wave of the Y2- plates on CRO screen, find the peak voltage (a). Note this value in the table-1.(This can be measured by connecting the CRO Y2-plates to the transformer secondary coil or directly to the carrier in.) Set the frequency of the audio signal to nearly 1 KHz and apply it to the base of T2 and adjust the time base of the CRO to observe at least two audio waves on the screen of the CRO. Also adjust the amplitude of the audio signal such that the audio wave in the modulated wave is completely observed on Y2-plates. Now the audio signal peak to peak voltage (2b) and the peak voltage (a) are measured from the Y1-plates and noted in table-1.

Now measure the maximum voltage (E_{cmax}) and minimum voltage (E_{cmin}) of the modulated signal from Y2-plates of CRO as shown in the Fig-3. Note them in the table-1. Repeat the experiment by changing the amplitude of the audio signal and note the values a, b, E_{cmax} and E_{cmin} in the <u>table-1</u>.

For demodulation, Y2-plates are disconnected from the secondary of the transformer. Now the secondary of the transformer is connected to demodulation circuit as in put. The out put of the demodulation circuit is connected to Y2-plates of CRO.

Now set the frequency (f_1) of in put audio signal to a convenient value and measure the time period and frequency (f_2) of the out put signal i.e. demodulated wave. These values are noted in the <u>table-2</u>. The experiment is repeated by changing the in put frequency. These frequency values $(f_1$ and $f_2)$ are found to be equal.

Similarly the amplitudes of the in put audio signal (b_1) and demodulated signals (b_2) can be compared as in the <u>table-3</u>. This part of the experiment is repeated by changing the amplitude of the in put audio signal (b_1) . The ratio $(b1/b_2)$ is found to be constant.

Precautions:-

- 1) Before going to the experiment the amplitude of the carrier wave measured.
- 2) The amplitude of the in put audio signal should not exceed the amplitude of the carrier signal.

Results:-

- 1) The modulation index at in put terminal and at the out put terminal are found to be equal in modulation.
- 2) The frequency of the in put audio signal and frequency of the demodulated wave are found to be equal.
- 3) The ratio of the amplitude of the in put audio signal and amplitude of the demodulated wave is found to be constant.

	<i>*</i>	Measu Peak to pe Voltage S Peak Volt	ement of ak (Vertical ensitivity. (nage a = (nxl)	eak vc mgth). (e of in	ı put signal (a) Divisions Volt/Div					
	W	Measurement of b	ofb		Measur	Measurement of E _{cmax}	стах	Measur	Measurement of E _{cmin}	cmin	$M_2 = $
S.No.	Peak to peak (Vertical) length. (Divisions)	Voltage Sensitivity. (Volt/Div)	Peak Voltage b = (nxl)/2 (volts)	$M_1 = \frac{b}{a}$	Peak to peak (Vertical) length. (Divisions)	Voltage Sensitivity. (Volt/Div)	E _{cmax} = (nxl) (volts)	Peak to peak (Vertical length). (Divisions)	Voltage Sensitivity. (Volt/Di	E _{cmin} = (nxl) (volts)	$\frac{E_{cmax} - E_{cmin}}{E_{cmax} + E_{cmin}}$

Tables for demodulation or detection

$\underline{\text{Table} - 2}$

Comparison of in put and out put frequencies

	In put applied	Measurer	ment of out put	frequency	
S.No.	frequency (f_1)	Peak to peak Horizontal length (l)	Time base (t)	Period T=(1 x t)	Frequency
	(Hz)	(Divisions)	Sec/div	Sec	$f_2 = \frac{1}{T} Hz$

Table - 3

Comparison of in put and out put amplitudes

			4 /	7			
	In	out amplitude b	1	Out p	out amplitude	b_2	
	Peak to peak	Voltage	Peak	Peak to peak	Voltage	Peak	
S.No.	(Vertical	Sensitivity.	Voltage	(Vertical	Sensitivity	Voltage	$\frac{b_1}{b_2}$
5.110.	length)	(Volt/Div)	$b_1=(nx1)/2$	length)	(Volt/Div)	$b_1=(nx1)/2$	b_2
	(Divisions)	(n)	(volts)	(Divisions)	(n)	(volts)	
	(1)			(1)			
	5						

* * * * *